VIVEKANANDA

COLLEGE OF ENGINEERING & TECHNOLOGY

(A Unit of Vivekananda Vidyavardhaka Sangha Puttur®)

NEHRU NAGAR, PUTTUR (D.K) -574 203,

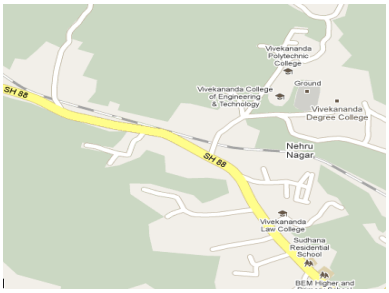
KARNATAKA STATE

Phone:**08251–234555, 235955 Fax:08251-236444**

Website: www.vcetputtur.ac.in, E-mail: principal@vcetputtur.ac.in

MANDATORY DISCLOSURES

Date: 20/October/2022

1	**AICTE File No.**	**South-West/1-10975684720/2022/EOA**	
	Date & Period of last approval	2022-2023	
2	**Name of the Institution**	**Vivekananda College of Engineering and Technology**	
	Address of the Institution	Nehru Nagar	
		Puttur–D.K.	
		574203	
		Karnataka	
	Longitude & Latitude	12-46-51-N	75-11-03-E
	Phone Number with STD code	08251–234555	
	FAX number with STD code	08251-236444	
	Office hours at the Institution	9.30–5.00	
	Academic hours at the institution	8.50–5.00	
	Email	principal@vcetputtur.ac.in	
	Website	www.vcetputtur.ac.in	
	Nearest Railway Station (dist. in KM)	Kabaka-Puttur	6
	Nearest Airport	Mangalore	60
3	**Type of Institution**	Private-Self Financed	
	Category(1)of the Institution	Non-Minority	
	Category(2)of the Institution	Co-education	

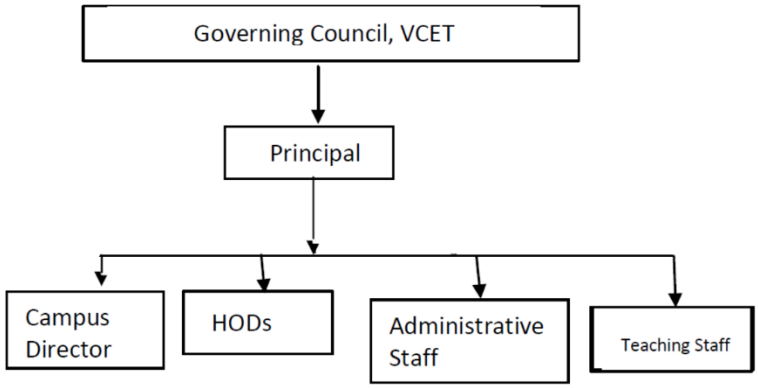
4	**Name of the organization Running the Institution**	Vivekananda Vidyavardhaka Sangha Puttur®
	Type of the organization	Society
	Address of the organization	Vivekananda College Campus, Neharu Nagara, PUTTUR, 574203
	Registered with	An act for the registration of Literary, Scientific and charitable
	Registration date	23/12/1915
	Website of the organization	www.vcetputtur.ac.in

5	**Name of the affiliating University**	Visvesvaraya Technological University (VTU)
	Address	"JnanaSangama", Belgavi, 590018
	Website	www.vtu.ac.in
	Latest affiliation period	2021-22

6	**Name of Principal/Director**	Dr. Mahesh Prasanna K
	Exact Designation	PRINCIPAL
	Phone number with STD code	08251-234555
	FAX number with STD code	08251-236444
	Email	principal@vcetputtur.ac.in
	Highest Degree	Ph.D
	Field of specialization	Implementation and Evaluation of Image Processing Algorithms Using Fuzzy Logic Controller

7	**Governing Board Members**	1. **Sri. K. Vishwas Shenoy** President 2. **Sri. T. S. Subrahmanya Bhat** Correspondent 3. **Sri. Muralidhara Bhat B.** Treasurer 4. **Sri. Ravikrishna D Kallaje** Director 5. **Dr. Suresh Putturaya** Director 6. **Sri. Santhosh Kuthamotte** Director 7. **Sri. Sathyanarayana B** Director 8. **Dr. Yashoda Ramachandra** Director 9. **Dr. Mahesh Prasanna K** Principal / Member Secretary 10. **Prof. Sowmya Anil** Staff representative
	Frequency of meetings & date of last meeting	Monthly. Last meeting on 23.09.2022

8	**Academic Advisory Committee**	1. Principal Chairman 2. HOD-CSE Member 3. HOD-Civil Member 4. HOD-ECE Member 5. HOD-Mechanical Member 6. HOD-AIMLE Member 7. HOD-CSE(DS) Member 8. HOD-Basic Science Member
	Frequency of meeting & date of last meeting	Once in a semester. 04/04/2022

9	**Organizational Chart**	

10	**Student feedback mechanism on Institutional Governance/ faculty performance**	An online portal has been designed to collect students' Feedback in two stages – Formative and Summative, once in every semester. Action taken report will be collected from faculty members if performance is poor in each and every parameter.

11	**Grievance redressal Mechanism for faculty, staff and students**	Students' grievances are looked into by the **Grievance Redressal Cell** consisting of Coordinator, Student Welfare Officer (SWO) and Student Counsellors lead by the principal. Faculty grievances are presented to the Governing Council by the staff representative.

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Academic Year 2022-23

VCET –Anti ragging Committee

Objectives:

1. To create an atmosphere of discipline by sending a clear message that no act of ragging shall be tolerated and any act of ragging shall not go unnoticed and unpunished.
2. To keep a continuous watch over ragging so as to prevent its occurrence and recurrence.
3. To promptly and strictly deal with the incidents of ragging brought to our notice.

Functional Responsibilities:

1. Displaying the boards stating evil nature, punishment of Ragging and also student's discipline.
2. Creation of cordial atmosphere in the campus.
3. Involving seniors and fresher's jointly in value based cultural and other activities.
4. Inter-action and casual warning to those who involves in ragging, ensuring the spot solutions by adapting soft measures.
5. In case of need, reporting to the nearest police station.

Committee Details:

Sl No.	Staff Name	Department	Contact No.
1	Dr. Mahesh Prasanna K	Principal	9945016992
2	Dr. Sekhar S Iyer	Director, MBA	9688618954
3	Dr. Manujesh B. J.	HOD, ME	9741729531
4	Dr. Anand V Rao	HOD, CV	9740546040
5	Prof. Krishna Mohana A.J.	HOD, CS	9844613782
6	Prof. SrikanthRao S. K.	HOD, ECE	9743703473
7	Dr. Govindaraj P	HOD, AI&ML, CD	9916578256
8	Dr. Vandana B.S.	Director, MCA	9448889152
9	Prof. M. Ramananda Kamath	HOD, BS	9740081411
10	Inspector of Police	Puttur Police Station	08251-230555

Naveen S P
Coordinator

Srikanth Rao S K
CSC-MS

Dr. Mahesh Prasanna K
Principal

PRINCIPAL
VIVEKANANDA COLLEGE OF ENGG.
& TECHNOLOGY, PUTTUR, D.K.-574203

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VCET – College Internal Complaints Committee (ICC)

2020 - 21

Objectives:

1. To create and ensure safe environment that is free of sexual harassment at the campus.
2. To create an atmosphere promoting equality and gender justice.
3. To create physical and social environment that will deter acts of sexual harassment.
4. To plan and carry out programmes for gender sensitization.

Functional Responsibilities:

1. To take up the complaints from the anti-sexual harassment squad and recommend the concerned authorities to follow up the same in a safe, accessible and sensitive manner.
2. To seek medical, police and legal intervention with the consent of complainant.
3. To make arrangements for appropriate psychological, emotional and physical support to the victims.

Committee Details:

Sl No.	Staff Name	Department	Role	Contact No.
1	Dr. Sowmya N J	Professor, CV	Chairman	9448725762
2	Smt. Roopa G K	Asst. Prof, CS	Convener	9980540800
3	Smt. Sesamma K S	SI of Police, Puttur	Member	9449615959
4	Sri. Ullas H	Advocate, Puttur	Member	8861880197
5	Dr. Deepak K B	Assoc. Prof, ME	Member	9483203087
6	Smt. Madhavi R Pai	Asst. Prof, FY	Member	9481264777
7	Sri. Ganesha K	Lab Instructor, CV	Member	8762129334
8	Sri. Shivaprasad H S	Foreman, ME	Member	9448313169
9	Kum. Vibha Nayak	Student, CS	Member	9783138943
10	Sri. Yatheesh K	Student, ME	Member	9740343489

11	Kum. Disha S	Student, EC	Member	7338029357
12	Sri. Anish Bangera	Student, CV	Member	8904875592
13	Kum. Shreedevi K S	Student, MBA	Member	8722171322

Convener | Chairman | CSC-MS | Principal

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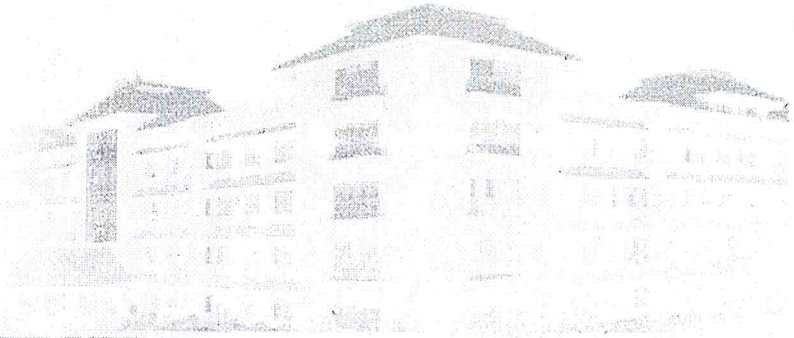
Office Order

Constitution of SC/ST/OBC committee (AY 2020-21)

As per the requirement of AICTE, the undersigned have constituted SC/ST/OBC committee with the following members.

1.	Sri. Achutha Prabhu K	Director, GC	Patron
2	Dr. Mahesh Prasanna	Principal	Chairman
3	Sri. Harish S R	Asst. Prof, ME	Convener
4	Dr. Sekhar S Iyer	Director, MBA	Member
5	Dr. Ananda V R	HoD, CV	Member
6	Dr. Manujesh B J	HoD, ME	Member
7	Dr. Harivinod N	HoD, CSE	Member
8	Sri. Shrikanth Rao. S K	HoD, ECE	Member
9.	Sri. Ramananda Kamath	HoD, FY	Member
10.	Sri. Prashantha Achar	Discipline Committee	Member
11.	Dr. Chethan P D	Student Welfare Officer	Member
12.	Smt. Roopa G K	Anti sexual harassment committee	Member

Principal
DR. MAHESH PRASANNA K.
PRINCIPAL
VIVEKANANDA COLLEGE OF ENGG
& TECHNOLOGY, PUTTUR, D.K. - 574



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Constitution of SC/ST/OBC cell (AY 2020-21)

As per the requirement of AICTE, the undersigned have constituted SC/ST/OBC cell with the following members .

Sl No.	Staff Name	Department	Contact No.	Role	Signature
1	Mr. Harish S R	ME	9449207667	Convener	
2	Mr. Satheesha Kumar K	ME	9449936366	Member	
3	Mr. Sumanth A	CV	9480761128	Member	
4	Mrs. Bhanupriya M P	CSE	7996311383	Member	
5	Mrs. Nisha G R	ECE	8971720836	Member	
6	Mrs. Shwethambika	FY	9449215221	Member	
7	Mrs. Reshma Pai	MBA	9844379977	Member	

The cell will monitor and endeavor to resolve issues/grievances related to SC/ST/OBC students at the institute level. It will perform its functions as per the guidelines and is informed to bring any issues in this regard to the notice of the undersigned for necessary actions. It is hereby notified for information of all concerned that the cell is constituted with effect from 21.09.2020

Principal

PRINCIPAL
VIVEKANANDA COLLEGE OF ENGG.
& TECHNOLOGY, PUTTUR, D.K.-574203

12	Name of the Department	Artificial Intelligence & Machine Learning Engineering	
	Course	Bachelor of Engineering	
	Level	Under Graduate	
	1st Year of approval by the Council	2021	
	Year wise Sanctioned Intake	60	60
	Year wise Actual Admissions	2021-22-63	2020–21-41
	Cutoff marks–General quota	45% in PCM	45 % in PCM
	% Students passed with Distinction	-	-
	% Students passed with First Class	-	-
	Students Placed	-	-
	Average Pay package, Rs./Year	-	-
	Students opted for Higher Studies	-	-
	Accreditation Status of the course	Not Eligible to apply	
	Doctoral Courses	Nil	
	Foreign Collaborations, if any	Nil	
	Professional Society Memberships	Nil	
	Professional activities Consultancy activities	Nil	
	Grants fetched	Nil	
	Departmental Achievements	Nil	
	Distinguished Alumni	Nil	

	Name of the Department	Computer Science & Engineering (Data Science)
	Course	Bachelor of Engineering
	Level	Under Graduate
	1st Year of approval by the Council	2022
	Year wise Sanctioned Intake	60
	Year wise Actual Admissions	2021-22-60
	Cutoff marks–General quota	45% in PCM
	% Students passed with Distinction	-
	% Students passed with First Class	-
	Students Placed	-
	Average Pay package, Rs./Year	
	Students opted for Higher Studies	-
	Accreditation Status of the course	Not Eligible to apply
	Doctoral Courses	Nil
	Foreign Collaborations, if any	Nil
	Professional Society Memberships	Nil
	Professional activities Consultancy activities	Nil
	Grants fetched	Nil
	Departmental Achievements	Nil
	Distinguished Alumni	Nil

	Name of the Department	Computer Science & Engineering		
	Course	Bachelor of Engineering		
	Level	Under Graduate		
	1st Year of approval by the Council	2001		
	Year-wise Sanctioned Intake	120	120	120
	Year-wise Actual Admissions	2021-22-121	2020-21-116	2019-20-121
	Cutoff marks–General quota	45% in PCM	45% in PCM	45% in PCM
	% Students passed with Distinction	2021-22–98%	2020-21–94.5%	2019-20–83%
	% Students passed with First Class	2021-22–2%	2020-21–2%	2019-20–15%
	Students Placed	2021-22–91	2020-21–70	2019-20-60
	Average Pay package, Rs. /Year	4,57,000/-	4,20,000/-	3,85,000/-
	Students opted for Higher Studies	-	1	-
	Accreditation Status of the course	Not Accredited		
	Doctoral Courses	Nil		
	Foreign Collaborations, if any	Nil		
	Professional Society Memberships	Nil		
	Professional activities Consultancy activities	Nil		
	Grants fetched	Nil		

	Departmental Achievements	1. Consistent and High Academic results. 2. Ms. Shraddha was honoured at VTU's 7th annual convocation with the Smt. Shwetha R Memorial Gold Medal Award. 3. Sneha shivanand Idurkar, 4th Rank, VTU Examinations – 2013. 4. Adarsh S P holds a Gold medal with meet record – Tripple Jump – inter University Athletics. 5. Suhas P M holds 2 Silver medal in Swimming at KHELO INDIA and also 1 gold, 8 silver and 1 bronze medal at VTU State level Swimming Competition – 2019-2020. 6. Lohith R N participated in VTU selection trials for men held at VTU Belagavi on 22nd, 23rd December 2021 and secured 1st place in 100 metres & 2nd place in 200 metres. 7. Lohith R N represented VTU in 81st All India Inter University Athletics meet – 2022 at Alvas, Moodabidre from 7th to 9th January 2022. 8. To encourage innovation and entrepreneurship among students, VCET, Puttur has established NAIN (New Age Innovation Network) center with financial support of Rs 1.20 crore over period of 3 three years from M/s. Karnataka Innovation and Technology Society (KITS), Govt of Karnataka. KITS has shortlisted 10 student projects under NAIN scheme for the year 2020-21. The ongoing three CS projects are; a) Smart energy meter using IoT technology – Rs. 2,90,000 sanctioned Amount b) Safety Alert device for Drowsy Driving Guide – Rs.2,80,000 sanctioned Amount c) Automatic Drone sprayer for agriculture - Rs.2,80,000 sanctioned Amount. 9. List of VGST funded projects (CS) a) Automatic Medicinal Plant Leaf Identification and Information System – Rs. 40000 10. List of KSCST funded projects (CS) a) Handbone Age Estimation – Rs. 5000 (2017-2018) b) Mobile Application for Automatic Identification of fall Armyworm (FAW) – Rs. 4500 (2019-2020) c) Android App Based Coffee Plant Disease Detection with Suggestive Remedies Using Machine Learning – Rs. 3500 (2020-21). 11. List of VTU funded projects (CS) 2018-19 a) IOT based Biometric authentication using edge computing – Rs. 5000 b) Children Safety monitoring using IOT – Rs. 5000. 2019-20 a) Early Detection of Brain Tumor Using Digital Image Processing – Rs. 5000 b) Automated Identification of Fall Army Worm – Rs. 5000.

	Distinguished Alumni	1. Mr. Sharath, The web people, Puttur, 2. Mr. Avanisha Krishna, Software Engineer, Diya System, 3. Mr. Praveen Udupa, Proprietor, A1 Logics. 4. Mr. Padmanabha E, Edakkana Traders, Puttur

	Name of the Department	Civil Engineering		
	Course	Bachelor of Engineering		
	Level	Under Graduate		
	1st Year of approval by the Council	2004		
	Year wise Sanctioned Intake	30	60	60
	Year wise Actual Admissions	2021–22- 18	2020 –21- 11	2019–20 -33
	Cut off marks– General quota	45% in PCM	45% in PCM	45% in PCM
	%Students passed with Distinction	2021 –22– 85%	2020 –21– 88%	2019–20 – 75.5%
	%Students passed with First Class	2021 –22– 6%	2020 –21– 7.5%	2019–20 – 19.5%
	Students Placed	2021 –22- 32	2020 –21- 4	2019–20 - 2
	Average Pay package, Rs./Year	2,50,000/-	3,92,000/-	5,73,000/-
	Students opted for Higher Studies	4	4	2
	Accreditation Status of the course	Accredited		
	Doctoral Courses	Yes–Ph.D (Part time registration)		
	Foreign Collaborations, if any	Nil		
	Professional Society Memberships	Life Member of Association of Consulting Civil Engineers (India)		
	Professional activities Consultancy activities	Yes (Innovation and Consultancy Cell in Department of Civil Engineering)		
	Grants fetched	Nil		
	Departmental Achievements	1. Consistent and High Academic results. 2. Department received 2nd, 3rd, 7th and 9th Rank in university level. 3. Best project of the year award in state level seminar and exhibition of student project program Organized by KSCST.		

	Distinguished Alumni	1. Dr. Arjun B M, Scientist, North-Eastern Space Applications Centre, Dept. of Space, GOI, 2. Dr. Akshatha Shetty, Prof and HOD, AJIT, Mangalore.

	Name of the Department	Electronics and Communication Engineering		
	Course	Bachelor of Engineering		
	Level	Under Graduate		
	1st Year of approval by the council	2001		
	Year-wise Sanctioned Intake	60	90	90
	Year-wise Actual Admissions	2021-22-61	2020-21-45	2019-20-76
	Cutoff marks–General quota	45% in PCM	45% in PCM	45% in PCM
	% Students passed with distinction	2021-22–99%	2020-21–95%	2019-20–74%
	% Students passed with First Class	2021-22-0%	2020-21-0%	2019-20–18.5%
	Students Placed	2021-22-54	2020-21-36	2019-20-17
	Average Pay package, Rs./Year	4,67,000/-	4,46,000/-	3,76,000/-
	Students opted for Higher Studies	-	1	5
	Accreditation Status of the course	Not Accredited		
	Doctoral Courses	Nil		
	Foreign Collaborations, if any	Nil		
	Professional Society Memberships	Nil		
	Professional activities Consultancy activities	Nil		
	Grants fetched	Nil		
	Departmental Achievements	1. Consistent and High Academic results 2. Overall 6th place in National level Solar Car Competition. 3. KSCST project fund is received. 4. First rank with 6 gold medals in VTU for Ms. Sindhura Saraswathi. 5. Mrs. Shriraksha K A secured Fourth rank in M.Tech (Digital electronics and communication systems.		

	Distinguished Alumni	1. Mr. Dileep Kudva, Sr Engineer, Dialog Semi-Conductors, USA. 2. Mrs. Sapna Thilak, Sr Engineer, Bosch, Bangalore. 3. Mr. Pramod Baliga, MTS Silicon Design Engineer, AMD Processor. 4. Mr. Mohammed Niyaz, Team Lead, Infosys, Mangalore.

	Name of the Department	Mechanical Engineering		
	Course	Bachelor of Engineering		
	Level	Under Graduate		
	1st Year of approval by the Council	2004		
	Year wise Sanctioned Intake	30	60	90
	Year wise Actual Admissions	2021-22-23	2020-21-18	2019-20-46
	Cutoff marks–General quota	45% in PCM	45% in PCM	45% in PCM
	% Students passed with Distinction	2021-22-98%	2020-21-90.5%	2019-20-83%
	% Students passed with First Class	2021-22-0%	2020-21-7.5%	2019-20-14%
	Students Placed	2021-22–28	2020-21–36	2019-20-33
	Average Pay package, Rs./Year	3,20,000/-	3,14,000/-	3,65,000/-
	Students opted for Higher Studies	1	1	-
	Accreditation Status of the course	Accredited		
	Doctoral Courses	Yes		
	Foreign Collaborations, if any	Nil		
	Professional Society Memberships	SAE/ISTE/IE		
	Professional activities Consultancy activities	Directorate of Cashew Research Campco India Limited, Puttur		
	Grants fetched	VTU-Research Grant – 7.0 Lakhs (2021)		

	Departmental Achievements	1. Consistent and High Academic results. 2. 3rd Rank in university level 2010-11 academic year. 3. The 5th Edition of the National Level SAE Aero-design Challenge was held at Erode, Coimbatore from 28th February to 1st March 2020, and "JATAYU AEROWING" designed and fabricated by Mechanical Engineering students received "Best Innovative Design" award. 4. The college team “REVAAN RACING” won the 1st place in National level SIEGER PRO KARTING CHAMPIONSHIP held at Adithya Group of Institutions, Kakinada, Andhra Pradesh between 13th to 17th February 2018. 5. For student projects, KSCST funding were awarded.
	Distinguished Alumni	1. Dr Jayavardhan, Education, DK. 2. Astron Chethan Lobo, Design, Nowleff. 3. Prasad Tonse, Engineer at Mercedes Benz 4. Kavan – Senior Product Design Engineer at Mercedes Benz 5. Mohandas K, AE, Water Authority Dept. Govt. of Karnataka 6. Sharath M L, Vigilance Officer, KSRTC 7. Seetharam Gowda, Dy. Manager, Oil & Gas Industry 8. Bhavith, Senior Engineer, Infosys

	Name of the Department	MCA
	Course	Master of Computer Application
	Level	Post Graduate
	1st Year of approval by the Council	2022
	Year wise Sanctioned Intake	60
	Year wise Actual Admissions	2021-22-54
	Cutoff marks–General quota	50% in UG
	% Students passed with Distinction	-
	% Students passed with First Class	-
	Students Placed	-
	Average Pay package, Rs./Year	-

	Students opted for Higher Studies	Nil
	Accreditation Status of the course	Not Eligible to apply
	Doctoral Courses	Nil
	Foreign Collaborations, if any	Nil
	Professional Society Memberships	Nil
	Professional activities Consultancy activities	Nil
	Grants fetched	Nil
	Departmental Achievements	Nil
	Distinguished Alumni	Nil

	Name of the Department	MBA		
	Course	Master of Business Administration		
	Level	Post Graduate		
	1st Year of approval by the Council	2007		
	Year wise Sanctioned Intake	60	60	60
	Year wise Actual Admissions	2021-22-60	2020-21-44	2019-20-44
	Cutoff marks–General quota	50% in UG	50% in UG	50% in UG
	% Students passed with Distinction	2020-21–50%	2020-21–50%	2019-20–44.64%
	% Students passed with First Class	2020-21-41.47%	2020-21-41.47%	2019-20-53.55%
	Students Placed	2021-22-20	2020-21-10	2019-20-5
	Average Pay package, Rs./Year	3,90,000/-	2,80,000/-	2,48,000/-
	Students opted for Higher Studies	Nil	Nil	Nil
	Accreditation Status of the course	Not Accredited		
	Doctoral Courses	Nil		

	Foreign Collaborations, if any	Nil
	Professional Society Memberships	Nil
	Professional activities Consultancy activities	Nil
	Grants fetched	Nil
	Departmental Achievements	1. Consistent and High Academic results. 2. Ms.Shama Pranamya won 2 Gold Medals in VTU Cultural Fest 2019 and 2020. 3. Mr.Mohammed Yusuf won Silver Medal in Decathlon and Javelin throw Gold Medal in 4x100 mtrs Relay in VTU Athletic meet 2018 & 2019.
	Distinguished Alumni	1. Sri. Rakesh Mayya, Actor, Color super TV Channel

Infrastructural Information

College Main Building

Krishna Chethana

Madhu Chethana

Inner View of College Block

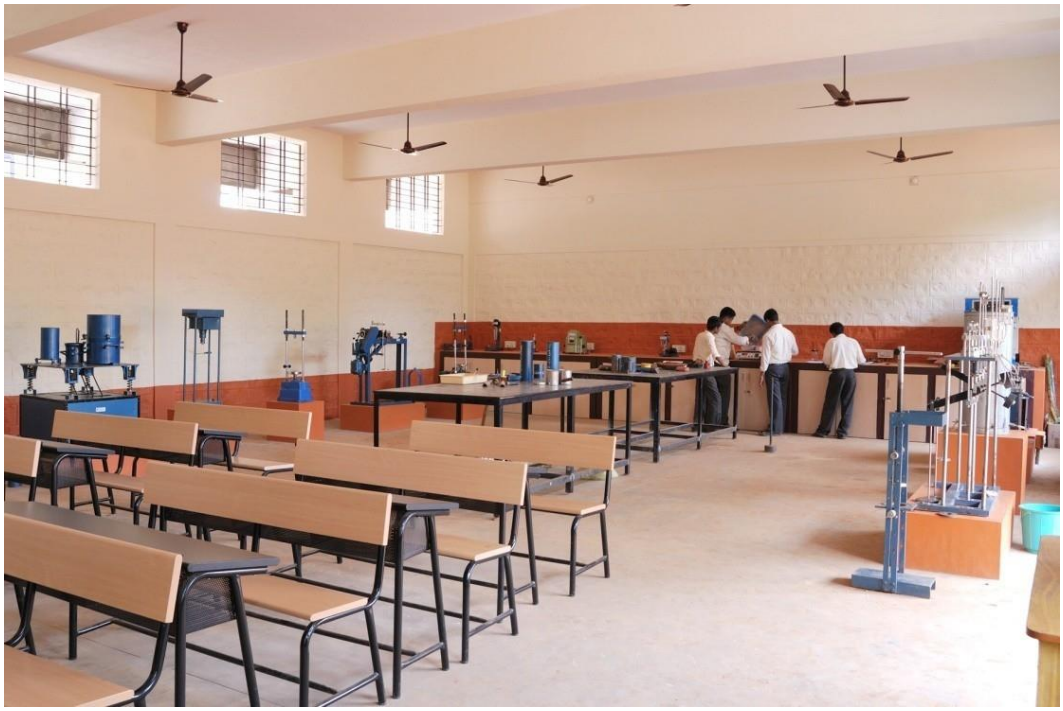
Classroom/Tutorial rooms

1) Laboratory details

a) Engineering Chemistry Lab

b) Analog Electronics Lab

c) Geo-Technical Lab



d) Machine Shop

e) Concrete Lab–Civil Engg

f) Environmental Engineering Lab

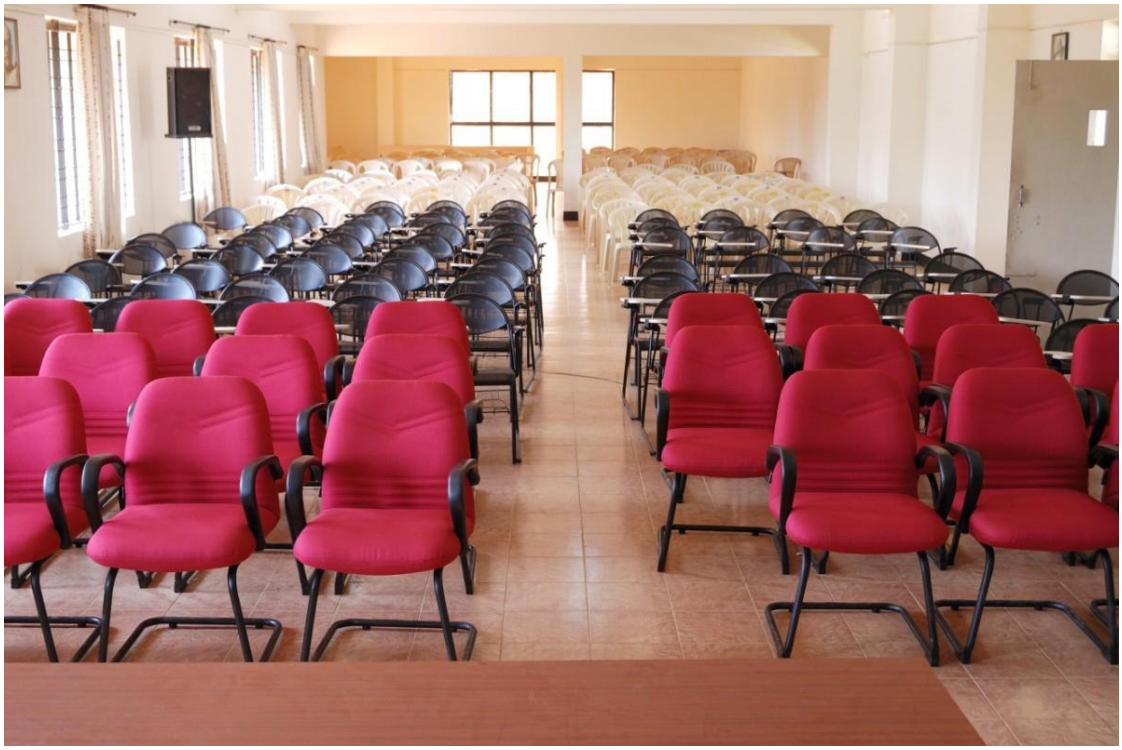
g) Fluid Mechanics Lab

h) Heat and Mass Transfer Lab–Mechanical Engineering

i) Material Testing Lab

j) Library

k) Seminar Hall



l) Canteen

m) Sports-Play Ground

n) Gymnasium

o) Girls Hostel

p) Boys Hostel

14	Admission quota	Govt. Quota	ComedK Quota	Management Quota
	Entrance Test/Admission Criteria	State CET	ComedK Test	Any Test
	Cutoff/last candidate admitted	45% in PCM	45% in PCM	45% in PCM
	Fees in Rupees	83,526	2,21,960	1,04,100
	No. of fee Waivers offered	Nil	Nil	Nil
	Admission Calendar	AUGUST	AUGUST	AUGUST
	PIO Quota	No	No	No

17	Academic Sessions	August to July
	Examination system, Year/Sem	Semester
	Period of declaration of results	February/March & June/July

18	Counseling/Mentoring	YES
	Career Counseling	YES
	Medical facilities	YES
	Student Insurance	YES

19	Students Activity Body	YES
	Cultural activities	YES
	Sports activities	YES
	Library activities	YES
	Magazine/Newsletter	YES
	Technical activities/Tech. Fest	YES
	Industrial Visits/Tours	YES
	Alumni activities	YES

20	Name of the Information Officer for RTI	Dr. Mahesh Prasanna K
	Designation	PRINCIPAL
	Phone number with STD code	9449104654, 08251-235955
	FAX number with STD code	08251-236444
	Email	principal@vcetputtur.ac.in

Name of the Teaching Staff	***Dr. Mahesh Prasanna K***		
Designation	Professor & Principal		
Department	Electronics and Communication Engineering		
Date of Joining the Institution	16/01/2015		
Qualifications with Class/Grade	UG-BE-FC/64%	PG–M.Tech-FCD/8.43	PhD-Yes
Total Experience in Years	Teaching–17Y	Industry -6Y	Research–NIL
Papers Published	National- NIL		International-12
Papers Presented in Conferences	National-3	International–5	
Ph.D Guide? Give field& University	Visvesvaraya Technological University/ ECE		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	Automation in VLSI Design		
Professional Memberships	ISTE (LM96055)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Dr Govindaraj P***
Designation	Associate Professor & Head
Department	AI and ML and Data science
Date of Joining the Institution	28/10/2021
Qualifications with Class/Grade	UG-BE-SC/60.2% PG–M.Tech-FC/69.10% PhD-YES
Total Experience in Years	Teaching–6Y Industry -0 Research–5Y
Papers Published	National- NIL International-05
Papers Presented in Conferences	National-NIL International–03
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM111058)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff:	***Mrs. Akshaya D. Shetty***
Designation:	Assistant Professor
Department:	Artificial Intelligence & Machine Learning
Date of Joining the Institution:	12/09/2022
Qualifications with Class/Grade:	UG-BE-FCD/74.82% PG–M.Tech-FCD/79.6% PhD- Registered (Comprehensive done)
Total Experience in Years:	Teaching–5Y3M Industry -1Y Research–Registered
Papers Published:	National- 1 International-8
Papers Presented in Conferences	National-1 International–8
Ph.D Guide? Give field& University:	NO/NIL
Ph.Ds/Projects Guided:	8
Books Published/IPRs/Patents:	NIL
Professional Memberships:	ISTE (Membership ID 122440)
Consultancy Activities:	NIL
Awards:	NIL
Grants fetched:	NIL
Interaction with Professional Institutions:	NIL

Name of the Teaching Staff	***Monica. K. P***
Designation	Assistant Professor
Department	Artificial Intelligence and Machine Learning
Date of Joining the Institution	10/10/2022
Qualifications with Class/Grade	UG-BE-FC/65% PG–M.Tech-FCD/9.02 CGPA PhD-NO
Total Experience in Years	Teaching–6Y Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Abhishek kumar K***		
Designation	Assistant Professor		
Department	Artificial Intelligence & Machine learning		
Date of Joining the Institution	28/08/2020		
Qualifications with Class/Grade	UG-BE-FC/61%	PG–M. Tech-FC/69%	PhD-NO
Total Experience in Years	Teaching–5Y	Industry -NIL	Research–NIL
Papers Published	National- NIL	International-NIL	
Papers Presented in Conferences	National-1	International–NIL	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM133934)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***AJAY SHASTRY C G***			
Designation	Assistant Professor			
Department	Artificial Intelligence & Machine Learning			
Date of Joining the Institution	01/07/2021			
Qualifications with Class/Grade	UG-BE-FC/60%	PG–M.Tech-FCD		PhD-NO
Total Experience in Years	Teaching–1Y6M	Industry -Nil	Research–NIL	
Papers Published	National- NIL		International-NIL	
Papers Presented in Conferences	National-1		International-NIL	
Ph.D Guide? Give field& University	NO/NIL			
Ph.Ds/Projects Guided	NA			
Books Published/IPRs/Patents	NIL			
Professional Memberships	ISTE (LM13395)			
Consultancy Activities	NIL			
Awards	NIL			
Grants fetched	NIL			
Interaction with Professional Institutions	NIL			

Name of the Teaching Staff	***Vaishnavi K V***
Designation	Assistant Professor
Department	AIML
Date of Joining the Institution	15/09/2022
Qualifications with Class/Grade	UG-BE-FC/66% PG–M.Tech-FCD/78% PhD-NO
Total Experience in Years	Teaching–9M Industry -2.4Y Research–NIL
Papers Published	National-2 International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Harshitha K***
Designation	Assistant Professor
Department	Data Science
Date of Joining the Institution	26/09/2022
Qualifications with Class/Grade	UG-BE-FC/62% PG–M.Tech-FCD/81% PhD-NO
Total Experience in Years	Teaching–6Y8M Industry -No Research–NIL
Papers Published	National- NIL International-Nil
Papers Presented in Conferences	National-Nil International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	No
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***AKHILA M L***		
Designation	Assistant Professor		
Department	CD		
Date of Joining the Institution	10/10/2022		
Qualifications with Class/Grade	UG-BE-FC/66.85%	PG–M.Tech-FCD/77.85%	PhD-NO
Total Experience in Years	Teaching–1Y6M	Industry -2Y9M	Research–NIL
Papers Published	National- NIL	International-NIL	
Papers Presented in Conferences	National-NIL	International–1	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM116814)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***KRISHNA MOHANA A J***
Designation	Assistant Professor & Head
Department	Computer Science & Engineering
Date of Joining the Institution	11/02/2019

Qualifications with Class/Grade	UG-BE-SC/ 56.84%	PG–M.Tech-FCD/ 9.01(CGPA)	PhD-NO
Total Experience in Years	Teaching–14Y	Industry -NIL	Research–NIL
Papers Published	National- NIL	International-NIL	
Papers Presented in Conferences	National-4	International–3	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM87798)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Uma K P***
Designation	Associate Professor
Department	Computer Science & Engineering
Date of Joining the Institution	24/08/2020
Qualifications with Class/Grade	UG-B.Sc-FC/62% PG–M.Tech-FCD/90 % PhD-YES
Total Experience in Years	Teaching–18Y Industry -0Y Research–NIL
Papers Published	National- 2 International-NIL
Papers Presented in Conferences	National-5 International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Dr. Jeevitha B K***
Designation	Associate Professor
Department	Computer Science Engineering
Date of Joining the Institution	28/08/2021
Qualifications with Class/Grade	UG-BE-SC/59.56% PG–M.Tech-FCD/74.5% PhD-Yes
Total Experience in Years	Teaching–1Y6M Industry -NIL Research-5Y
Papers Published	National- NIL International-4
Papers Presented in Conferences	National-NIL International–3
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE IEEE (93689290) ORCID (0000-0002-9114-3503)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Roopa G K***
Designation	Assistant Professor
Department	Computer Science & Engineering
Date of Joining the Institution	20/08/2005
Qualifications with Class/Grade	UG-BE-FCD/74% PG–M.Tech-FCD/82% PhD-NO
Total Experience in Years	Teaching–17Y Industry-0Y Research–NIL
Papers Published	National- 4 International-8
Papers Presented in Conferences	National-1 International–0
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117054)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***BHARATHI K***		
Designation	Assistant Professor		
Department	Computer Science & Engineering		
Date of Joining the Institution	28/01/2008		
Qualifications with Class/Grade	UG-BE-FC/67%	PG–M.Tech-FCD/72%	PhD-NO
Total Experience in Years	Teaching–14Y7M	Industry- NIL	Research–NIL
Papers Published	National- NIL		International-5
Papers Presented in Conferences	National-NIL	International–NIL	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM117052)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Radhika Shetty D S***			
Designation	Assistant Professor			
Department	CSE			
Date of Joining the Institution	28/01/2008			
Qualifications with Class/Grade	UG-BE-FCD/71.6%	PG–M.Tech-FCD/79%		PhD-NO
Total Experience in Years	Teaching–14Y7M		Industry -NIL	Research–NIL
Papers Published	National-Nil		International-05	
Papers Presented in Conferences	National-Nil		International-Nil	
Ph.D Guide? Give field& University	NO			
Ph.Ds/Projects Guided	NA			
Books Published/IPRs/Patents	Nil			
Professional Memberships	ISTE (LM117053)			
Consultancy Activities	NIL			
Awards	NIL			
Grants fetched	NIL			
Interaction with Professional Institutions	NIL			

Name of the Teaching Staff: ***SAVITHA M***

Designation	Assistant Professor		
Department	CSE		
Date of Joining the Institution	30/09/2022		
Qualifications with Class/Grade	UG-BE-SC/59%	PG–M.Tech-FCD/8.90 CGPA	PhD-NO
Total Experience in Years	Teaching–15Y	Industry -NIL	Research–NIL
Papers Published	National- NIL	International-3	
Papers Presented in Conferences	National-NIL	International–1	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM117058)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Mr. Pradeep Kumar K G***
Designation	Assistant Professor
Department	Computer Science & Engineering
Date of Joining the Institution	15/11/2021
Qualifications with Class/Grade	UG-BE-FC/62% PG–M.Tech-FCD/72% PhD-NO
Total Experience in Years	Teaching–12Y9M Industry -NIL Research–6Y
Papers Published	National- 1 International-10
Papers Presented in Conferences	National-1 International–4
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	IAENG (143544) IACSIT (8034911) CSTA (2223107)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Mohan A R***
Designation	Assistant Professor
Department	CSE
Date of Joining the Institution	28/06/2022
Qualifications with Class/Grade	UG-BE-FC/70.59% PG–M.Tech-FCD/76% PhD-NO
Total Experience in Years	Teaching – 12Y7M Industry - NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National- NIL International– NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM57562)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Swapnalaxmi K***		
Designation	Assistant Professor		
Department	Computer Science & Engineering		
Date of Joining the Institution	20/08/2020		
Qualifications with Class/Grade	UG-BE-FC/64%	PG–M.Tech-FCD/74%	PhD- Pursuing
Total Experience in Years	Teaching–10Y5M	Industry -10M	Research–NIL
Papers Published	National- NIL	International-NIL	
Papers Presented in Conferences	National-2	International–1	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM 96054)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Pramod Kumar P M***
Designation	Assistant Professor
Department	CSE
Date of Joining the Institution	18/07/2012
Qualifications with Class/Grade	UG-BE-SC/57% PG–M.Tech-FCD/72% PhD-NO
Total Experience in Years	Teaching–10Y2M Industry -NIL Research–NIL
Papers Published	National- NIL International-5
Papers Presented in Conferences	National-1 International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117056)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***SHWETHA C H***
Designation	Assistant Professor
Department	CSE
Date of Joining the Institution	27/08/2020
Qualifications with Class/Grade	UG-BE-FC/67% PG–M.Tech-FCD/78% PhD-NO
Total Experience in Years	Teaching–8Y Industry -1Y6M Research–NIL
Papers Published	National- NIL International-2
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM133932)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Raghavendra T K***
Designation	Assistant Professor
Department	Computer Science and Engineering
Date of Joining the Institution	27/09/2021

Qualifications with Class/Grade	UG-BE-FC/63%	PG–M.Tech-FCD/73%	PhD-NO
Total Experience in Years	Teaching–6Y 9M	Industry -Nil	Research–NIL
Papers Published	National- 02	International-02	
Papers Presented in Conferences	National-Nil	International–02	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs	Nil		
Patents	01		
Professional Memberships	ISTE (LM117061)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***THAPASWINI P S***		
Designation	Assistant Professor		
Department	CSE		
Date of Joining the Institution	15/07/2016		
Qualifications with Class/Grade	UG-BE-FC/68.31%	PG–M.Tech-FCD/77%	PhD-NO
Total Experience in Years	Teaching–7Y	Industry -0	Research–NIL
Papers Published	National- NIL	International-NIL	
Papers Presented in Conferences	National-1	International–1	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM117069)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***DEEPTHI M B***		
Designation	Assistant Professor		
Department	Computer Science Engineering		
Date of Joining the Institution	20/08/2020		
Qualifications with Class/Grade	UG-BE-FC/67.5%	PG–M.Tech-FCD/9.41CGPA	PhD-NO
Total Experience in Years	Teaching–3Y	Industry -1Y1M	Research–NIL
Papers Published	National- NIL	International-1	
Papers Presented in Conferences	National-NIL	International–2	
Ph.D Guide? Give field& University	NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM133931)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***SHRINIDHI A***			
Designation	Assistant Professor			
Department	Computer Science			
Date of Joining the Institution	15/09/2022			
Qualifications with Class/Grade	UG-BE-FC/60.22%	PG–M.Tech-FCD/9.34(CGPA)		PhD-NO
Total Experience in Years	Teaching–3Y2M	Industry -1Y	Research–NIL	
Papers Published	National- NIL	International-NIL		
Papers Presented in Conferences	National-NIL	International–NIL		
Ph.D Guide? Give field& University	NO/NIL			
Ph.Ds/Projects Guided	NA			
Books Published/IPRs/Patents	NIL			
Professional Memberships	NIL			
Consultancy Activities	NIL			
Awards	NIL			
Grants fetched	NIL			
Interaction with Professional Institutions	NIL			

Name of the Teaching Staff	***MANOHAR JHA***
Designation	Assistant Professor
Department	COMPUTER SCIENCE & ENGG.
Date of Joining the Institution	30/08/2022
Qualifications with Class/Grade	UG-BE-FC/63% PG–M.Tech-FCD/69% PhD-NO
Total Experience in Years	Teaching–2Y Industry -NO Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-0 International–0
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NA
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Jayashree M***
Designation	Assistant Professor
Department	Computer Science Engineering
Date of Joining the Institution	20/08/2020
Qualifications with Class/Grade	UG-BE-FC/68% PG–M.Tech-FCD/82.25% PhD-NO
Total Experience in Years	Teaching–2Y Industry -NIL Research–NIL
Papers Published	National- NIL International-1
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Manasa P***
Designation	Assistant Professor
Department	CS
Date of Joining the Institution	20/08/2020
Qualifications with Class/Grade	UG-BE-FCD/71% PG–M.Tech-FCD/79% PhD-NO
Total Experience in Years	Teaching–2Y Industry -0Y Research–NIL
Papers Published	National- 1 International-1
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Priyanka M Yalagach***
Designation	Assistant Professor
Department	CSE
Date of Joining the Institution	04/07/2022
Qualifications with Class/Grade	UG-BE-FC/64% PG–M.Tech-FCD/8.1CGPA PhD-NO
Total Experience in Years	Teaching–1Y Industry -2Y Research–NIL
Papers Published	National- 2 International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Dr. Ananda V R***
Designation	Professor & Head
Department	Civil Engineering
Date of Joining the Institution	01/08/2020
Qualifications with Class/Grade	UG-BE-FCD/79.50% PG–MTech-FCD/80% PhD-Yes
Total Experience in Years	Teaching–15Y Industry -2y Research–NIL
Papers Published	National- NIL International-05
Papers Presented in Conferences	National-2 International–4
Ph.D. Guide? Give field& University	Yes/Civil Engineering- Construction Technology & Structural Engineering
Ph.Ds./Projects Guided	01 Ongoing
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE, MICI, MIE, MIGS
Consultancy Activities	NIL
Awards	01
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff`	***Dr. Sowmya N J***
Designation	Professor
Department	Civil Engineering
Date of Joining the Institution	05/07/2017
Qualifications with Class/Grade	UG-BE-FCD/72% PG–M.Tech-FCD/71% PhD-FC
Total Experience in Years	Teaching–21Y7M Industry -0 Research–10Y
Papers Published	National- 3 International-15
Papers Presented in Conferences:	National-3 International–3
Ph.D Guide? Give field	Geotechnical and Transportations Engineering University: VTU Belagavi NO:5
Ph.Ds /Projects Guided	UG: 50 , PG: 15
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM116814), IRC
Consultancy Activities	Soil and water testing, material testing, third party inspection works.
Awards held at	Best paper award in the 2013 received at IRC-national conference Guhawati, Assam. Best project award in the 2022 received from KSCST, Karnataka.
Grants fetched	VGST, KFIST-L2 of Rs 40 lakhs in 2019 ATAL FDP of Rs 0.93 lakhs 3 grants from KSCST for students' projects
Interaction with Professional Institutions	Yes [NITK Surathkal, Vidyavardhaka college of Engineering Mysore, UVCE Bangalore, Mangalore University, CPCRI Kasaragod and IISC Bangalore].

Name of the Teaching Staff	***Shivarama M S***
Designation	Associate Professor
Department	Civil Engineering
Date of Joining the Institution	15/07/2011
Qualifications with Class/Grade	UG-BE-SC/59% PG–M.Tech-FCD/80% PhD-No
Total Experience in Years	Teaching–23Y7M Industry -6Y Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-2 International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117035)
Consultancy Activities	Involved in Department Consultancy Activities
Awards	NIL
Grants fetched	KSCST Student Project Grants
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Prashantha***
Designation	Assistant Professor
Department	Civil Engineering
Date of Joining the Institution	05/11/2005
Qualifications with Class/Grade	UG-BE-FC/78% PG–MTech-FCD/8.3 CGPA PhD-NO
Total Experience in Years	Teaching–16Y10M Industry -1y Research–NIL
Papers Published	National- 04 International-NIL
Papers Presented in Conferences	National-8 International–1
Ph.D. Guide? Give field& University	NO/NIL
Ph.Ds./Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM116814)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***SUBRAHMANYA R M***
Designation	Assistant Professor
Department	CIVIL ENGINEERING
Date of Joining the Institution	31/07/2009
Qualifications with Class/Grade	UG-BE-FC/68.8% PG–M.Tech-FCD/85.7% PhD-NO
Total Experience in Years	Teaching–13Y2M Industry -3M Research–5Y7M
Papers Published	National- 02 International-03
Papers Presented in Conferences	National-02 International–02
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117036)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***SUREKHA T***
Designation	Assistant Professor
Department	Civil Engineering
Date of Joining the Institution	01/07/2015
Qualifications with Class/Grade	UG-BE-FC/76.97% PG–M.Tech-FCD/85.57% PhD-NO
Total Experience in Years	Teaching–10Y Industry -NIL Research–NIL
Papers Published	National- NIL International-1
Papers Presented in Conferences	National-1 International–NIL
Ph. D Guide? Give field& University	NO/NIL
Ph. Ds/ Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117043)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***JAYAKRISHNA BHAT D***
Designation	Assistant Professor
Department	CIVIL ENGINEERING
Date of Joining the Institution	30/09/1988
Qualifications with Class/Grade	UG-BE-FC/70.33% PG–M.Tech-FCD/81.63% PhD-NO
Total Experience in Years	Teaching–10Y2M Industry -NIL Research–NIL
Papers Published	National- NIL International-1
Papers Presented in Conferences	National-1 International–2
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117037), ICI (10788)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***SHISHIRAKRISHNA S***
Designation	Assistant Professor
Department	Civil Engineering
Date of Joining the Institution	05/08/2022
Qualifications with Class/Grade	UG-BE-FCD/73.8% PG–M.Tech-FCD-85.88% PhD-NO
Total Experience in Years	Teaching–12Y Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-3 International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds / Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117041)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Sumanth A***
Designation	Assistant Professor
Department	Civil Department
Date of Joining the Institution	15/07/2013
Qualifications with Class/Grade	UG-BE-65% PG–M.Tech-74.4% PhD-Pursuing
Total Experience in Years	Teaching–11Y Industry -NIL Research–6Y
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-2 International–1
Ph.D Guide? Give field& University	NO
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117038)
Consultancy Activities	NIL
Awards	Received best presentation award for the international conference paper Hydrological Modeling of the Upper Cauvery River Basin Using SWAT, held at NIT Rourkela.
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***RAJESHA R***		
Designation	Assistant Professor		
Department	Civil Engineering		
Date of Joining the Institution	08/08/2016		
Qualifications with Class/Grade	UG-B.Sc-SC/59%	PG–M.Sc-FC/69%	PhD-Pursuing
Total Experience in Years	Teaching–10Y	Industry -4M	Research–3Y
Papers Published	National-02	International-01	
Papers Presented in Conferences	National-04	International–03	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM7051)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***PREETHAM GANESH***
Designation	Assistant Professor
Department	Civil Engineering
Date of Joining the Institution	28/08/2020
Qualifications with Class/Grade	UG-BE-FC/60.26% PG–M.Tech-FCD/8.31CGPA PhD-NO
Total Experience in Years	Teaching–2Y Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph. D Guide? Give field& University	NO/NIL
Ph.Ds/ Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***VIDYASHREE P S***
Designation	Assistant Professor
Department	Civil Engineering
Date of Joining the Institution	24/08/2020
Qualifications with Class/Grade	UG-BE-FCD/75.41% PG–M.Tech-FCD/78.83% PhD-NO
Total Experience in Years	Teaching–2Y Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph. D Guide? Give field& University	NO/NIL
Ph. Ds/ Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Narasimha Pai***		
Designation	Assistant Professor		
Department	Civil Engineering		
Date of Joining the Institution	25/08/2020		
Qualifications with Class/Grade	UG-BE-FC	PG–M.Tech-FCD	PhD-NO
Total Experience in Years	Teaching–2Y	Industry -NIL	Research–NIL
Papers Published	National- NIL	International-NIL	
Papers Presented in Conferences	National-NIL	International–NIL	
Ph. D Guide? Give field& University	NO/NIL		
Ph. Ds/ Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	NIL		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Raveesh L R***
Designation	Assistant Professor
Department	Civil Engineering
Date of Joining the Institution	24/08/2020

Qualifications with Class/Grade UG-BE-FC PG–M.Tech-FCD PhD-NO

Total Experience in Years Teaching–2Y Industry -NIL Research–NIL

Papers Published National- NIL International-NIL

Papers Presented in Conferences National-NIL International–NIL

Ph. D Guide? Give field& University NO/NIL

Ph. Ds/ Projects Guided

NA

Books Published/IPRs/Patents NIL

Professional Memberships NIL

Consultancy Activities NIL

Awards NIL

Grants fetched NIL

Interaction with Professional Institutions NIL

Name of the Teaching Staff	***Shrikanth Rao S.K***		
Designation	Assistant Professor		
Department	Electronics and Communication		
Date of Joining the Institution	07/08/2006		
Qualifications with Class/Grade	UG-BE-FC	PG–M.Tech-FCD	PhD-Pursuing
Total Experience in Years	Teaching–16Y	Industry -1Y2M	Research–NIL
Papers Published	National- 3		International-5
Papers Presented in Conferences	National-4	International–6	
Ph.D Guide? Give field& University	NO		
Ph.Ds/ Projects Guided	25		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE(LM117012)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Dr. Mahantesh R. Choudhari***
Designation	Associate Professor
Department	Electronics & Communication
Date of Joining the Institution	24/08/2020
Qualifications with Class/Grade	UG-BE-SC/58% PG–M.Tech-FCD/78.20% PhD-First/74%
Total Experience in Years	Teaching–6Y7M Industry -4Y Research–3Y
Papers Published	National-4 International-6
Papers Presented in Conferences	National-7 International–4
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	1
Professional Memberships	IFERP(PM27819064), TIE B'lore (FEBBGM2021), IAENG(276408)
Consultancy Activities	Founder & Director: MARC Edu-Tech Solutions (Reg.)
Awards	Business Award-2020 (MSME), Many Regional Awards (Karnataka)
Grants fetched	5,00,000
Interaction with Professional Institutions	15+

Name of the Teaching Staff	***Rajani Rai B***		
Designation	Assistant Professor		
Department	Electronics and Communication		
Date of Joining the Institution	23/08/2005		
Qualifications with Class/Grade	UG-BE-FCD	PG–M.Tech-FCD	PhD-Pursuing
Total Experience in Years	Teaching–17Y	Industry -0Y	Research–NIL
Papers Published	National- 1	International-1	
Papers Presented in Conferences	National-1	International–1	
Ph.D Guide? Give field& University	NO		
Ph.Ds/Projects Guided	4		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM117032) IEEE (94251549)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Sowmya Anil***
Designation	Assistant Professor
Department	Electronics & Communication
Date of Joining the Institution	06/08/2006
Qualifications with Class/Grade	UG-BE-FC/69% PG–M.Tech-FCD/76% PhD-NO
Total Experience in Years	Teaching–16Y Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-1 International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117013)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***PRABHA G S***
Designation	Assistant Professor
Department	Electronics & Communication
Date of Joining the Institution	01/08/2007
Qualifications with Class/Grade	UG-BE-FC/68.58% PG–M.Tech-FC/64% PhD-Registered
Total Experience in Years	Teaching–16Y Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-2 International–2
Ph.D Guide? Give field& University	NO
Ph.Ds/Projects Guided	NO
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117014), IEEE(95611775)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***VENKATESH Y C***
Designation	Assistant Professor
Department	ELECTRONICS AND COMMUNICATION ENGG.
Date of Joining the Institution	27/09/2022
Qualifications with Class/Grade	UG-BE-FC/66% PG–M.Tech-FC/66% PhD-PURSUING
Total Experience in Years	Teaching–12Y2M Industry -0Y Research–3Y
Papers Published	National- 1 International-02
Papers Presented in Conferences	National-1 International–02
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Shivaprasad***
Designation	Assistant Professor
Department	EC
Date of Joining the Institution	22/07/2014
Qualifications with Class/Grade	UG-BE-SC/59% PG–M.Tech-FC/68% PhD-Pursuing
Total Experience in Years	Teaching–10Y7M Industry -1Y Research–NIL
Papers Published	National- 1 International-3
Papers Presented in Conferences	National-2 International–3
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	1
Professional Memberships	ISTE (LM117023)
Consultancy Activities	Undertakes B.E/M.Tech internship, project guidance at Tech-Graylogix, Mlore Undertakes B.E/M.Tech internship, project guidance at Marc-Edutech, Blore
Awards	Completed E-yantra TBT with grade A
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Nirupama K***		
Designation	Assistant Professor		
Department	EC		
Date of Joining the Institution	20/07/2012		
Qualifications with Class/Grade	UG-BE-FCD/77%	PG–M.Tech-FC/69%	PhD-NO
Total Experience in Years	Teaching–10Y2M	Industry -7M	Research–NIL
Papers Published	National- NIL	International-NIL	
Papers Presented in Conferences	National-3	International–NIL	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM117031)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

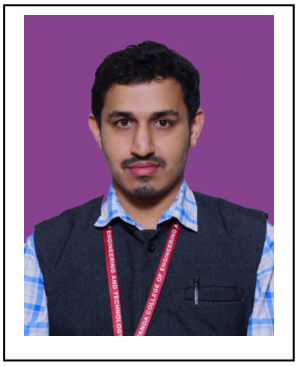
Name of the Teaching Staff	***Mahabaleshwara Bhat P***		
Designation	Assistant Professor		
Department	Electronics and Communication		
Date of Joining the Institution	17/06/2015		
Qualifications with Class/Grade	UG-BE-FC/67.85%	PG–M. Tech-FCD/77.63%	PhD-Pursuing
Total Experience in Years	Teaching–10Y2M	Industry -NIL	Research–NIL
Papers Published	National- NIL	International-1	
Papers Presented in Conferences	National-3	International–2	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM117034)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Naveena C***
Designation	Assistant Professor
Department	Electronics & Communication
Date of Joining the Institution	23/07/2014
Qualifications with Class/Grade	UG-BE-FC/63.5% PG–M.Tech-FCD/80% PhD-Pursuing
Total Experience in Years	Teaching–8Y3M Industry -NIL Research–NIL
Papers Published	National- NIL International-1
Papers Presented in Conferences	National-5 International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM116814), IAENG (289089)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Nisha G R***		
Designation	Assistant Professor		
Department	ECE		
Date of Joining the Institution	25/07/2014		
Qualifications with Class/Grade	UG-BE-FCD/71%	PG–M.Tech-FCD/78%	PhD-Pre Registered
Total Experience in Years	Teaching–8Y3M	Industry -NIL	Research–NIL
Papers Published	National- NIL	International-NIL	
Papers Presented in Conferences	National-4	International–2	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM117022)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***SHREYAS H.***
Designation	Assistant Professor
Department	ECE
Date of Joining the Institution	18/10/2021
Qualifications with Class/Grade	UG-BE-FCD/72% PG–M.Tech-FCD/76% PhD-NO
Total Experience in Years	Teaching–6Y10M Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-4 International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117027)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***SHRUTHI P R***
Designation	Assistant Professor
Department	ECE
Date of Joining the Institution	20/08/2020
Qualifications with Class/Grade	UG-BE-FC/70.48% PG–MTech-FCD/71.2% PhD-NO
Total Experience in Years	Teaching–3Y8M Industry -0Y Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-1 International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	Won third place in national level paper presentation on “copy move forgery detection of color and grey images using image hashing” held at SJBIT Bangalore.
Grants fetched	NIL
Interaction with Professional Institutions	NIL

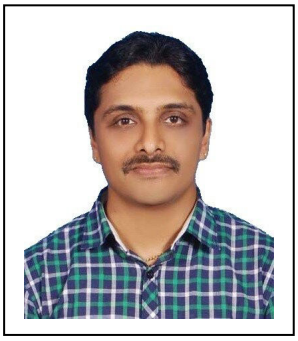


Name of the Teaching Staff	***AKSHAY S P***
Designation	Assistant Professor
Department	EC
Date of Joining the Institution	20/08/2020
Qualifications with Class/Grade	UG-BE-FC/65% PG–M.Tech-FCD/8.65cgpa PhD-NO
Total Experience in Years	Teaching–2Y Industry -0Y Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Shriraksha K A***
Designation	Assistant Professor
Department	EC
Date of Joining the Institution	27/08/2020
Qualifications with Class/Grade	UG-BE-FCD/75% PG–M.Tech-FCD/84.6% PhD-NO
Total Experience in Years	Teaching–2Y Industry -0Y Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Dr. Manujesh B J***
Designation	Professor & Head
Department	Mechanical Engineering
Date of Joining the Institution	29/06/2017
Qualifications with Class/Grade	**UG-BE- FCD / 76.8% PG – M.Tech -FCD / 82.05% PhD -Yes**
Total Experience in Years	**Teaching–18Y7M Industry - NIL Research–6 Years**
Papers Published	National- 03 International-11
Papers Presented in Conferences	National-03 International–04
Ph.D Guide? Give field& University	Yes / Mechanical Engineering - VTU
Ph.Ds/Projects Guided	05/19-UG & 09-PG
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (**LM46314**)
Consultancy Activities	Yes
Awards	NIL
Grants fetched	NAIN- 2.90 Lakhs, VTU-RGS-7.0 Lakhs
Interaction with Professional Institutions	NRCC, NITK-Surathkal

Name of the Teaching Staff	***Dr. Deepak KB***
Designation	Associate Professor
Department	Mechanical Engineering
Date of Joining the Institution	07/06/2006
Qualifications with Class/Grade	UG-BE-FC/62.76% PG–M.Tech-FCD/77.45% Ph.D-YES
Total Experience in Years	Teaching–17Y2M Industry -0 Research–06Y
Papers Published	National-05 International-06
Papers Presented in Conferences	National-05 International–08
Ph.D Guide? Give field& University	NO
Ph.Ds/Projects Guided	25
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM116814), IRED, IAENG(168919), IFERP
Consultancy Activities	YES, City Municipal Council, Puttur
Awards	YES, Best KSCST Project of the year, Best paper presentation at International Conference.
Grants fetched	YES, KSCST, VTU student project, NAIN
Interaction with Professional Institutions	YES, International Conference organizing committee, technical talk, Judge for project expo.



Name of the Teaching Staff	***SUDARSHAN M L***
Designation	Assistant Professor
Department	MECHANICAL ENGINEERING
Date of Joining the Institution	07/08/2006
Qualifications with Class/Grade	UG-BE-FC/68% PG–M.Tech-FCD/82% PhD-NO
Total Experience in Years	Teaching–16Y2M Industry -NIL Research–NIL
Papers Published	National- 16 International-03
Papers Presented in Conferences	National-10 International–02
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM52228)
Consultancy Activities	Puttur, Municipality Activity
Awards	NIL
Grants fetched	KSCST, Rotary India
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***HARISH S R***
Designation	**Assistant Professor**
Department	**Mechanical Engineering**
Date of Joining the Institution	**27/08/2007**
Qualifications with Class/Grade	UG-**BE-FC/68%** PG–**M.Sc (Engg)- FC** PhD-NO
Total Experience in Years	Teaching–**17**Y**6**M Industry -NIL Research–**6**Y
Papers Published	National- **02** International-**03**
Papers Presented in Conferences	National-**05** International– **06**
Ph.D Guide? Give field & University	NO
Ph.Ds/Projects Guided	**15 [UG]**
Books Published/IPRs/Patents	NIL
Professional Memberships	**ISTE [LM117074], IAENG [171614]**
Consultancy Activities	**1. ICAR- Directorate Cashew Research - Puttur** **2. TMC-Puttur**
Awards	NIL
Grants fetched	**1. VTU Student Project**
Interaction with Professional Institutions	**Expert talk at Govt. PU College, Kombettu**

Name of the Teaching Staff	***SATHEESHA KUMAR K***
Designation	Assistant Professor
Department	MECHANICAL ENGINEERING
Date of Joining the Institution	20/07/2010
Qualifications with Class/Grade	UG-BE-FC/65.17% PG–M.Tech-FCD/86% PhD-NO
Total Experience in Years	Teaching– 13Y Industry -NIL Research–NIL
Papers Published	National- 1 International- 4
Papers Presented in Conferences	National- 12 International– 4
Ph.D Guide? Give field& University	NO/NIL
~~Ph.Ds~~/Projects Guided	12 [UG]
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117083), IAENG (291852)
Consultancy Activities	ICAR-DCR
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	Expert talk at Govt. PU College Kombettu, Puttur D K

Name of the Teaching Staff	***Naveenakrishna P V***
Designation	Assistant Professor
Department	Mechanical Engineering
Date of Joining the Institution	16/07/2012
Qualifications with Class/Grade	UG-BE-SC/59% PG–M.Tech-FCD/76% PhD-NO
Total Experience in Years	Teaching–10Y Industry -NIL Research–NIL
Papers Published	National- 2 International- 2
Papers Presented in Conferences	National-4 International–2
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM80150), IAENG (215539)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Mr. Naveen S.P.***
Designation	Assistant Professor
Department	Mechanical Engineering
Date of Joining the Institution	16/07/2012
Qualifications with Class/Grade	UG-BE-FC/62% PG–M.Tech-FCD/77% PhD-NO
Total Experience in Years	Teaching–10Y2M Industry -4M Research–NIL
Papers Published	National- 11 International-2
Papers Presented in Conferences	National-2 International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	8(UG)
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM80149), IAENG-231400
Consultancy Activities	TMC PUTTUR
Awards	NIL
Grants fetched	NAIN, VTU STUDENT PROJECT
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***AJITH K***
Designation	Assistant Professor
Department	Mechanical Engineering
Date of Joining the Institution	15/07/2011
Qualifications with Class/Grade	UG-BE-FCD/76.2% PG–M.Tech-FCD/75.3% PhD-NO
Total Experience in Years	Teaching–9Y3M Industry -NA Research–NA
Papers Published	National- 1 International-1
Papers Presented in Conferences	National-4 International–2
Ph.D Guide? Give field& University	NO/NIL
Projects Guided	13
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117086)
Consultancy Activities	NIL
Awards	i) Best Project of the year award by KSCST in the year 2020-21 ii) Best Innovative Design Award in National Level Manovegam event in the year 2020-21
Grants fetched	NAIN, KSCST
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Deepak Kumar Shetty K***
Designation	Assistant Professor
Department	Mechanical Engineering
Date of Joining the Institution	10/06/2015
Qualifications with Class/Grade	UG-BE-FC/65.8% PG–M.Tech-FCD/83.3% PhD-NO
Total Experience in Years	Teaching–7Y3M Industry -3Y5M Research–NIL
Papers Published	National-2 International-NIL
Papers Presented in Conferences	National-1 International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117089)
Consultancy Activities	"Simulation of load cell system" was submitted on 16/02/2017 to Supram Industries, Bengaluru
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Raghavendra Prasad S.A***
Designation	Assistant Professor
Department	Mechanical Engineering
Date of Joining the Institution	30/09/2021
Qualifications with Class/Grade	UG-BE-FC/68% PG–M. Tech-FCD/82% PhD-NO
Total Experience in Years	Teaching–6Y7M Industry -NA Research–NA
Papers Published	National- 0 International-8
Papers Presented in Conferences	National-0 International–0
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds / Projects Guided	NIL
Books Published /IPRs/ Patents	NIL
Professional Memberships	1. MISTE 2. Review committee member of IJRAR journals since June 2020. Membership ID: 116266
Consultancy Activities	NIL
Awards	Nil
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Ranjith Shetty K***		
Designation	Assistant Professor		
Department	Mechanical Engineering		
Date of Joining the Institution	01/02/2021		
Qualifications with Class/Grade	UG-BE-FC	PG–M. Tech-FCD	PhD-NO
Total Experience in Years	Teaching–1Y6M	Industry -NA	Research–NA
Papers Published	National- 0		International-0
Papers Presented in Conferences	National-1		International–1
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds / Projects Guided	NIL		
Books Published /IPRs/ Patents	NIL		
Professional Memberships	NIL		
Consultancy Activities	NIL		
Awards	Nil		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Rajesh A R***		
Designation	Assistant Professor		
Department	Mechanical Engineering		
Date of Joining the Institution	01/02/2021		
Qualifications with Class/Grade	UG-BE-SC	PG–M.Sc-FC	PhD-NO
Total Experience in Years	Teaching–1Y6M	Industry -NA	Research–NA
Papers Published	National- 0	International-8	
Papers Presented in Conferences	National-0	International–0	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds / Projects Guided	NIL		
Books Published /IPRs/ Patents	NIL		
Professional Memberships	ISTE		
Consultancy Activities	NIL		
Awards	Nil		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***M RAMANANDA KAMATH***
Designation	Associate Professor & Head
Department	Basic Science (Mathematics)
Date of Joining the Institution	25/07/2016
Qualifications with Class/Grade	UG-B.SC-FCD/71.13% PG–M.Sc.-FC/61.76% PhD-NO
Total Experience in Years	Teaching–27Y Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM 117102)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	VGST GRANTS OF Rs. TWO LAKHS
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Thejaswini L P***
Designation	Assistant Professor
Department	Physics (BS)
Date of Joining the Institution	15/04/2004
Qualifications with Class/Grade	UG-B.Sc-FC/68.33% PG–M.Sc-FCD/71.2% PhD-NO
Total Experience in Years	Teaching–21Y6M Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM52231)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Ms. LATHA MOHAN SHETTY***
Designation	Assistant Professor
Department	Basic Science (Humanities)
Date of Joining the Institution	10/10/2013
Qualifications with Class/Grade	UG-B.Com-SC/53.56% PG–MA-FC/64.5% PhD-NO
Total Experience in Years	Teaching–19Y8M Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	Technical English-I, Pristine Publishing House, Urma, Mangaluru (ISBN: 978-81-937838-8-7)
Professional Memberships	ISTE (LM117108)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Ms. Vandana Shankar***		
Designation	Assistant Professor		
Department	Basic Science (Humanities& Placement and Training Department)		
Date of Joining the Institution	01/08/2007		
Qualifications with Class/Grade	UG-B.Com-FC	PG–MBA-FC	PhD-NO
Total Experience in Years	Teaching–19Y	Industry -NIL	Research–NIL
Papers Published	National- NIL	International-NIL	
Papers Presented in Conferences	National-NIL	International–NIL	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	NIL		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	Yes, with Corporate		

Name of the Teaching Staff	***Shwethambika P.***
Designation	Assistant Professor
Department	Chemistry
Date of Joining the Institution	10/06/2011
Qualifications with Class/Grade	UG-BSc-FCD/90.7% PG–MSc-FCD/79.2% PhD-Pursuing
Total Experience in Years	Teaching–14Y Industry -NIL Research–NIL
Papers Published	National- NIL International-04
Papers Presented in Conferences	National-3 International–3
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117105)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Dr. Chethan P.D.***		
Designation	Assistant Professor		
Department	Chemistry		
Date of Joining the Institution	15/07/2013		
Qualifications with Class/Grade	UG-BSc-FC/71%	PG–M.Sc-FC/65%	PhD-Yes
Total Experience in Years	Teaching–9Y2M	Industry -NIL	Research–2 years
Papers Published	National- NIL		International-04
Papers Presented in Conferences	National-1	International–2	
Ph.D Guide? Give field& University	NO		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE(LM117106)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Nikhila T***
Designation	Assistant Professor
Department	Chemistry
Date of Joining the Institution	16/09/2022

Qualifications with Class/Grade	UG-BSc-FCD/87.78%	PG–MSc-FCD/7.6cgpa	PhD-NO
Total Experience in Years	Teaching–NIL	Industry -0Y	Research–NIL
Papers Published	National- NIL		International-NIL
Papers Presented in Conferences	National-NIL		International–NIL
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	NIL		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	**MADHAVI R PAI**		
Designation	Assistant Professor		
Department	MATHEMATICS		
Date of Joining the Institution	15/07/2013		
Qualifications with Class/Grade	UG-B.Sc-FC/80%	PG–M.Sc-FC/63%	PhD-NO
Total Experience in Years	Teaching–9Y2M	Industry -NIL	Research–NIL
Papers Published	National- NIL		International-NIL
Papers Presented in Conferences	National-NIL		International–NIL
Ph.D Guide? Give field & University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM 117107)		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Ravishankar N K***
Designation	Assistant Professor
Department	Basic Science -Mathematics
Date of Joining the Institution	31/01/2014
Qualifications with Class/Grade	UG-Bsc-PME-FCD 81.3% PG–M.sc(Mathematics)-FC 63.5 PhD-NO
Total Experience in Years	Teaching–9.2Y Industry NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117109)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Dr. Raveesha P.M.***
Designation	Assistant Professor
Department	Basic Science (Physics)
Date of Joining the Institution	16/03/2022
Qualifications with Class/Grade	UG (B.Sc.)-60.88%, B.Ed. -78.9% PG–M.Sc. (Physics) 72.88% PhD-Yes
Total Experience in Years	Teaching–6 years Industry -NIL Research–5 years
Papers Published	International-4 Conference Proceedings-2
Papers Presented in Conferences	National-6 International–3
Ph.D Guide? Give field& University	Dr. Ganesh Sanjeev, Professor of Physics in Mangalore University Field: Radiation processing of materials
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	DAE-BRNS sponsored Junior Research Fellowship under the research project entitled by ***"Radiation effects on polymer nano-composites"***
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***RESHMA***
Designation	Assistant Professor
Department	Basic Science (Mathematics)
Date of Joining the Institution	12/09/2022
Qualifications with Class/Grade	UG-BSc-FCD/ 85% PG–MSc-FCD/89% PhD-NO
Total Experience in Years	Teaching–6Y Industry -NIL Research–3Y
Papers Published	National- NIL International-1
Papers Presented in Conferences	National-NIL International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***SHREESHARANYA U R***
Designation	Assistant Professor
Department	MATHEMATICS
Date of Joining the Institution	20/08/2020
Qualifications with Class/Grade	B.Sc./87 % M.Sc./77 % PhD-NO
Total Experience in Years	Teaching–3Y2M Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Santhoshkumar M***
Designation	Assistant Professor
Department	Basic Science -Physics
Date of Joining the Institution	20/08/2020
Qualifications with Class/Grade	UG-B.Ed -FCD PG–M.sc(Physics)-FC PhD-NO
Total Experience in Years	Teaching–2Y Industry NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Sneha B S***
Designation	Assistant Professor
Department	Basic Science -Chemistry
Date of Joining the Institution	31/07/2020
Qualifications with Class/Grade	UG-Bsc-FC 76.66% PG–M.Sc(Chemistry)-FCD 70% PhD-NO
Total Experience in Years	Teaching–2Y Industry NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National - 4 International–NIL
Ph.D Guide? Give field& University	NO
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Dr.Vandana B.S***
Designation	Associate Professor & Head
Department	MCA
Date of Joining the Institution	20/01/2021
Qualifications with Class/Grade	UG-BSc/74%% PG–M.Tech-FCD/8.88 PhD-YES
Total Experience in Years	Teaching–15Y10M Industry -NIL Research–6Y
Papers Published	National- NIL International-9
Papers Presented in Conferences	National-0 International–3
Ph.D Guide? Give field& University	NO
Ph.Ds/Projects Guided	NO
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM86477)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Vasudeva Shenoy U***		
Designation	Assistant Professor		
Department	MCA		
Date of Joining the Institution	25/08/2022		
Qualifications with Class/Grade	UG-B.Sc.-FC/64.2%	PG–M.C.A-FCD/76.34%	PhD-NO
Total Experience in Years	Teaching–19Y	Industry -0Y	Research–NIL
Papers Published	National- NIL	International-NIL	
Papers Presented in Conferences	National- NIL	International– NIL	
Ph.D Guide? Give field& University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	NIL		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Shylesh B C***		
Designation	Assistant Professor		
Department	MCA		
Date of Joining the Institution	25/10/2021		
Qualifications with Class/Grade	UG-B.Sc.-SC/54.80%	PG–MCA-FCD/75.87%	PhD-NO
Total Experience in Years	Teaching–14Y4M	Industry -2Y Research–2Y	
Papers Published	National- NIL	International-2	
Papers Presented in Conferences	National-3	International–3	
Ph.D Guide? Give field & University	NO/NIL		
Ph.Ds/Projects Guided	NA		
Books Published/IPRs/Patents	NIL		
Professional Memberships	ISTE (LM58419), LM IAENG (272394), SM ICDRC, Professional Member IFERP		
Consultancy Activities	NIL		
Awards	NIL		
Grants fetched	NIL		
Interaction with Professional Institutions	NIL		

Name of the Teaching Staff	***Ramesh K***
Designation	Assistant Professor
Department	MCSA
Date of Joining the Institution	25/07/2022
Qualifications with Class/Grade	UG-BE-FC/68% PG–M.Tech-FCD/78% PhD-NO
Total Experience in Years	Teaching–5Y Industry -3Y Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-2 International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM116814)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Arpana T J***
Designation	Assistant Professor
Department	MCA

Date of Joining the Institution	01/12/2021
Qualifications with Class/Grade	UG - BCA - FC/68% PG - MCA -FCD/78% PhD-NO
Total Experience in Years	Teaching – 8M Industry - 3.6Y Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International-NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Neema H***
Designation	Assistant Professor
Department	MCA
Date of Joining the Institution	25/10/2021
Qualifications with Class/Grade	UG-BCA-FCD/91% PG–MCA-FCD/88%
Total Experience in Years	Teaching–1Y Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Mr. Giridhar C P***
Designation	Assistant Professor
Department	M.C.A.
Date of Joining the Institution	14/09/2022
Qualifications with Class/Grade	UG-BCA-FCD/83.5% PG–M.MCA-FCD/8.7% PhD-NO-NA
Total Experience in Years	Teaching–NIL Industry -NIL Research–NIL
Papers Published	National- NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***DR SEKHAR S IYER***
Designation	Professor & Director
Department	MBA
Date of Joining the Institution	27/03/2017
Qualifications with Class/Grade	UG-BBM-Dist. And Rank PG–MBA – FC PhD- Completed
Total Experience in Years	Teaching– 18Y7M Industry -22Y Research–3Y (Part time)
Papers Published	National- NIL International- 4
Papers Presented in Conferences	National- 1 International–2
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	MBA Students' Projects guided
Books Published/IPRs/Patents	NIL
Professional Memberships	National Institute of Personal Membership
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	Board of Advisor- All India corporate council for Skill development

Name of the Teaching Staff	***DR BHARGAV S V RAMACHANDRA***
Designation	Associate Professor
Department	MBA
Date of Joining the Institution	20/08/2020
Qualifications with Class/Grade	UG-B.Sc-FC PG–MBA – SC PhD- Completed
Total Experience in Years	Teaching– 18Y6M Industry -22Y Research–4Y (Part time)
Papers Published	National- NIL International- 10
Papers Presented in Conferences	National- NIL International–12
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	7 Guided scholars awarded Ph.D
Books Published/IPRs/Patents	NIL
Professional Memberships	Asian Management Association, Chennai Quality Circle Forum India, Bangalore TQM International Forum, Mysore
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Dr. Robin Manohar Shinde***
Designation	Associate Professor
Department	MBA
Date of Joining the Institution	01/08/2022
Qualifications with Class/Grade	UG-BSc-FC/65%, PG–MBA-FCD/70%, PG–MHRM-FC/60% MPhil-YES, PhD-YES, NET-YES
Total Experience in Years	Teaching–14Y Industry -3Y Research–12Y
Papers Published	National- 04 International-07
Papers Presented in Conferences	National-14 International–09
Ph.D Guide? Give field& University	YES/MANAGEMENT - SRINIVAS UNIVERSITY
Ph.Ds/Projects Guided	5
Books Published/IPRs/Patents	NIL
Professional Memberships	NHRD, MMA, III
Consultancy Activities	NIL
Awards	NIL
Grants fetched	Rs. 50,000 (Insurance Institute of India for PhD)
Interaction with Professional Institutions	BOS, BOE Member for Autonomous Institutions and Universities

Name of the Teaching Staff	***RAKESH M***
Designation	Assistant Professor
Department	MBA
Date of Joining the Institution	11/09/2009
Qualifications with Class/Grade	UG-BBM-FC/61% PG–MBA - FC/63% PhD- Pursuing
Total Experience in Years	Teaching– 14Y3M Industry -NIL Research–4 Yrs (Part time)
Papers Published	National- NIL International- 3
Papers Presented in Conferences	National- 2 International–2
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	MBA Students Projects guided
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117097)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***ASHLEY D'SOUZA***
Designation	Assistant Professor
Department	MBA
Date of Joining the Institution	17/07/2012
Qualifications with Class/Grade	UG-B.COM-FC/62.64% PG–MBA - FC/63.28% PhD- Pursuing
Total Experience in Years	Teaching– 10Y3M Industry -5Y 9M Research–4 Yrs (Part time)
Papers Published	National- NIL International- NIL
Papers Presented in Conferences	National- 1 International–1
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	MBA Students' Projects guided
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117095)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Guyton Lobo***
Designation	Assistant Professor
Department	MBA
Date of Joining the Institution	01.08.2009
Qualifications with Class/Grade	UG-BBM – 50% PG–MBA-60% PhD-NO
Total Experience in Years	Teaching–13Y7M Industry -05Y Research–NIL
Papers Published	National- 2 International-Nill
Papers Presented in Conferences	National-Nill International–Nill
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***RESHMA PAI A***
Designation	Assistant Professor
Department	MBA
Date of Joining the Institution	20/01/2011
Qualifications with Class/Grade	UG-BBM-FCD/71.5% PG–MBA-FC/69.63% PhD-NO
Total Experience in Years	Teaching–11Y8M Industry -NIL Research–NIL
Papers Published	National- 3 International-2
Papers Presented in Conferences	National-2 International–3
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117099)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	NIL
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***JEEVITHA B V***
Designation	Assistant Professor
Department	MBA
Date of Joining the Institution	17/07/2012
Qualifications with Class/Grade	UG-BSc-FC/68.1% PG–MBA-FC/6.48CGPA PhD-NO
Total Experience in Years	Teaching–10Y2M Industry -NIL Research–NIL
Papers Published	National- 3 International-2
Papers Presented in Conferences	National-2 International–3
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	ISTE (LM117101)
Consultancy Activities	NIL
Awards	NIL
Grants fetched	
Interaction with Professional Institutions	NIL

Name of the Teaching Staff	***Balachandra Gowda B***
Designation	Physical Education Director
Department	Physical Education
Date of Joining the Institution	16/07/2016
Qualifications with Class/Grade	UG-B.P.Ed-FC PG–M.P.Ed-FC PhD-NO
Total Experience in Years	Teaching–18Y6M Industry -NIL Research–NIL
Papers Published	National-NIL International-NIL
Papers Presented in Conferences	National-NIL International–NIL
Ph.D Guide? Give field& University	NO/NIL
Ph.Ds/Projects Guided	NA
Books Published/IPRs/Patents	NIL
Professional Memberships	NIL
Consultancy Activities	NIL
Awards	NIL
Grants fetched	
Interaction with Professional Institutions	NIL

KARNATAKA EXAMINATIONS AUTHORITY

PROVISIONAL FEES STRUCTURE – 2022-23

Engineering Fee Structure – 2022

COURSE	COLLEGE TYPE	CATEGORIES				
		GM, 2A, 2B, 3A, 3B (1. Including SC / ST income above 10.00 Lakhs. 2. Including CAT-1 above 2.5 Lakhs) (In ₹.)	SNQ (Engineering Courses) (In ₹.)	SC / ST (In ₹.)		CAT-1 Income below 2.5 Lakhs (In ₹.)
				Income up to Rs.2.50 Lakhs	Income up to Rs.10.00 Lakhs	
1	2	3	4	5	6	7
ENGINEERING / ARCHITECURE	Government	38,200/-	21,700/-	500/-	21,700/-	21,700/-
	Aided courses In Aided colleges	38,200/-	21,700/-	500/-	21,700/-	21,700/-
	Un-aided colleges including Minority (Type-1) and Un-Aided courses In Aided colleges	91,796/-	31,110/-	500/-	31,110/-	75,296/-
	Un-aided colleges including Minority (Type-2) and Un-Aided courses In Aided colleges	98,984/-	31,110/-	500/-	31,110/-	82,484/-
	Deemed / Private University	91,796/-	-	500/-	31,110/-	75,296/-
B.PHARMA	Government	14,530/-	-	500/-	6,000/-	6,000/-
	Un-aided colleges	26,500/-	-	500/-	6,000/-	17,970/-
PHARM-D	Un-aided colleges	67,500/-	-	500/-	5,200/-	67,500/-
Farm Sc. Courses (Per Semester)	Government	29,810/-	-	500/-	15,155/-	29,810/-
B.V.Sc	Government	53,170/-	-	9,460/-	9,460/-	16,550/-
B.F.Sc (Fisheries & Dairy)	Government	29,170/-	-	11,790/-	11,790/-	15,410/-

COURSE	University Fees (Included in Fees in above table)
ENGINEERING	10,610/-
ARCHITECURE	11,260/-
B.PHARMA	5,500/-
PHARM-D	4,700/-

NOTE:

1. For Architecture course apart from the above fees Rs.650/- is extra.
2. ₹.20,000/- as other fees is included in the above table, for Unaided and Private/Deemed universities engineering colleges.
3. ₹.10,000/- as other fees is included in the above table, for Government and Aided engineering colleges.

VIVEKANANDA COLLEGE OF ENGG. AND TECHNOLOGY, NEHRU NAGAR, PUTTUR

LIST OF STUDENTS WHO ARE ELIGIBLE FOR FEE CONCESSION/SCHOLORSHIP

SL. NO	USN	SRUDENT NAME	FATHER NAME	COURSE	CET RANK	PU OVERALL %	ADMISSION TYPE	INSTITUTE LAST PASSED	PERIOD: 2021-22				
									%	SCHOLORSHIP	FEE CONCESSION	ELIGIBILITY CRITERIA	REMARKS
18-19/01	4VP18EC004	AKANKSHA PANGAL	YOGESH PANGAL	EC	17218		CET	VIVEKANANDA PU COLLEGE, PUTTUR	V SEM - 8.44 VI SEM - 9.00 **CGPA - 8.89**	30,000.00		1. VIVEKANANDA PU STUDENT 2. CGPA ≥ 8.85 & < 9.35	
19-20/01	4VP19CS029	DHARITHRI	SUBRAHMANYA KUMAR	CS	11911		CET	VIVEKANANDA PU COLLEGE, PUTTUR	III SEM - 8.13 IV SEM - 8.79 **CGPA - 9.01**	30,000.00		1. VIVEKANANDA PU STUDENT 2. CGPA ≥ 8.85 & < 9.35	
19-20/02	4VP19CS079	SANTHRUPTHI S	SURESH G	CS	15283		CET	VIVEKANANDA PU COLLEGE, PUTTUR	III SEM - 8.42 IV SEM - 9.04 **CGPA - 9.00**	30,000.00		1. VIVEKANANDA PU STUDENT 2. CGPA ≥ 8.85 & < 9.35	
									TOTAL	**90,000.00**	-		

Annexure IV

Abstract for the 1st Year B.E Admission made during 2020-21 (KEA+COMED-K+MANAGEMENT)

Name of the Institution: **Vivekananda College of Engineering and Technology, Puttur**

Sl. No.	Name of the Course	Intake	SC		ST		CAT-I		IIA		IIB		IIIA		IIIB		GM		PH		SNQ		371J		J&K		PIO		Foreign Nationals		TOTAL		Admitted
			Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	Boy	Girl	
1	Artificial Intelligence & Machine Learning	60	-	-	1	-	-	-	2	1	1	-	2	-	1	-	20	10	-	-	2	1	-	-	-	-	-	-	-	-	29	12	41
2	Computer Science & Engineering	120	-	1	2	2	1	3	1	10	1	2	1	10	7	4	33	27	-	-	2	4	-	-	-	-	-	-	-	-	48	63	111
3	Civil Engineering	60	-	-	-	-	-	-	-	-	-	-	-	-	-		7	1	-	-	2	1	-	-	-	-	-	-	-	-	9	2	11
4	Electronics & Communication Engineering	90	-	-	3	1	-	-	6	1	1	-	2	1	-	2	17	7	-	-	-	4	-	-	-	-	-	-	-	-	29	16	45
5	Mechanical Engineering	60	-	-	2	-	-	-	2	-	-	-	2	-	-	-	7	1	-	-	3	-	-	-	-	-	-	-	-	-	16	1	17
	Total	390	-	1	8	3	1	3	11	12	3	2	7	11	8	6	84	46	-	-	9	10	-	-	-	-	-	-	-	-	131	94	225

13.03.2021

PRINCIPAL 13/03/21

Dr. Mahesh Prasanna K
PRINCIPAL
VIVEKANANDA COLLEGE OF
ENGINEERING & TECHNOLOGY
Puttur - 574203, D.K. DIST.

Annexure - II

Name of the College: **Vivekananda College of Engineering and Technology, Puttur** **Academic Year : 2021-22**

Total Intake of all the Course: **360 + 18 (SNQ)**

Sl. No.	Course	KEA (A)					Comed-K (B)			Management (C)									Total (A+B+C)		
		KEA General			SNQ					Management			COMEDK Unfilled Seats			KEA Unfilled Seats					
		Intake	Admission	Vacancy	Seats	Admission	Intake	Admission	Vacancy	Intake	Admission	Vacancy	Unfilled Seats	Admission	Vacancy	Unfilled Seats	Admission	Vacancy	Intake	Admission	Vacancy
1	ARTIFICIAL INTELLIGENCE AND MACHINE LEARNIG	27	23	4	3	3	18	0	18	15	15	0	18	18	0	4	4	0	60	**60**	0
	COMPUTER SCIENCE AND ENGINEERING (DATA SCIENCE)	27	23	4	3	3	18	0	18	15	15	0	18	18	0	4	1	3	60	**57**	3
2	COMPUTER SCIENCE AND ENGINEERING	54	49	5	6	6	36	1	35	30	30	0	35	35	0	5	0	5	120	**115**	5
3	CIVIL ENGINEERING	14	4	10	2	2	9	0	9	7	7	0	9	5	4	10	0	10	30	**16**	14
4	ELECTRONICS AND COMMUNICATION ENGINEERING	27	24	3	3	3	18	0	18	15	15	0	18	18	0	3	0	3	60	**57**	3
5	MECHANICAL ENGINEERING	13	5	8	1	1	9	0	9	8	8	0	9	9	0	8	0	8	30	**22**	8
		162	**128**	**34**	**18**	**18**	**108**	**1**	**107**	**90**	**90**	**0**	**107**	**103**	**4**	**34**	**5**	**29**	**360**	**327**	**33**

Total No. of Admission: **327 + 18** Total No. of Vacancies: **33**

Date: 31/03/2022

Principal

Dr. Mahesh Prasanna K.
PRINCIPAL
VIVEKANANDA COLLEGE OF
ENGINEERING & TECHNOLOGY
Puttur - 574203, D.K. DIST.

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
("ವಿ ಟಿ ಯು ಅಧಿನಿಯಮ ೧೯೯೪" ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ)
VISVESVARAYA TECHNOLOGICAL UNIVERSITY
(State University of Government of Karnataka Established as per the VTU Act, 1994)
"JnanaSangama" Belagavi-590018, Karnataka, India

Prof. Dr. B. E. Rangaswamy, Ph.D.
REGISTRAR(I/C)

Phone: (0831) 2498100
Fax : (0831) 2405467

REF: VTU/BGM/ACA/2022-23/ 4197

DATE: 19 NOV 2022

Revised-NOTIFICATION

Subject: - Revised-Academic Calendar of 1st[d] semesters of B.E./B.Tech./B.Arch./B.Plan., programs of University regarding...
Reference: The Hon'ble Vice-Chancellor's approval dated: 18.11.2022

The revised-academic calendar concerned to 1st semester of B.E./B.Tech./B.Arch./B.Plan., programs of University for academic year 2022-23 are hereby notified as mentioned below;

Revised Academic Calendar for I Semester of UG programs for the Academic Year 2022-23 (Tentative)			
Details	**I semester B.E./B.Tech.**	**I semester B.Arch.**	**I semester B.Plan**
**Induction Program	01.12.2022 To 10.12.2022	01.12.2022 To 10.12.2022	01.12.2022 To 10.12.2022
Commencement of I semester Classes	12.12.2022	12.12.2022	12.12.2022
Last Working day of I Semester	31.03.2023	31.03.2023	31.03.2023
Practical Examinations	03.04.2023 To 14.04.2023	03.04.2023 To 14.04.2023	03.04.2023 To 14.04.2023
Theory Examinations	17.04.2023 To 10.05.2023	17.04.2023 To 10.05.2023	17.04.2023 To 10.05.2023
Commencement of II Semester	15.05.2023	15.05.2023	15.05.2023

Please Note:

- The academic sessions for ODD semesters should commence on the **date mentioned** above.

** **Induction Program** shall be conducted for 10 days at the beginning of 1st semester and 11 days at the beginning of the 2nd semester.

During the induction program, college must brief about the new curriculum implemented from the academic year 2022-23.

- The Institute needs to function for **six days** a week with Saturday being half a working day. #if required, the college can also plan to have extra classes on Saturday afternoons and Sundays full day to complete academic activities within the duration mentioned.
- The faculty/staff shall be available to undertake any work assigned by the university.
- Notification regarding the Calendar of Events relating to the conduct of University **Examinations** will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar **may be modified** based on guidelines/directions issued in the future by MHRD/UGC/AICTE/State Government.
- Academic Calendar is also applicable for **Autonomous Colleges.** If any changes are to be effected by Autonomous Colleges in the academic terms and examination schedule, they could do so with the approval of the University.
- AICTE Activity point details circular will be issued by the Registrar's office separately.
- If any clarification/correction, please email to - **sbhvtuso@yahoo.com**

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges, Chairpersons of the University departments are hereby informed to bring the academic calendar to the notice of all concerned.

Sd/-

REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The chairperson, of the Department of Mechanical Engineering /Civil Engineering /Computer Science and Engineering, Electronics & Communication Engineering of the University.

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information.
3. Special Officer QPDS VTU Belagavi for information
4. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
5. The Director I/c. ITI SMU, VTU Belagavi for information and to make arrangements to upload Academic Calendar on the VTU web portal.
6. The Director of Physical Education, VTU Belagavi for information
7. OS for information and make arrangements to send the circular regarding AICTE Activity Points
8. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

19/11/22

REGISTRAR

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
("ವಿ ಟಿ ಯು ಅಧಿನಿಯಮ ೧೯೯೪" ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ)
VISVESVARAYA TECHNOLOGICAL UNIVERSITY
(State University of Government of Karnataka Established as per the VTU Act, 1994)
"JnanaSangama" Belagavi-590018, Karnataka, India

REGISTRAR

Phone : (0831) 2498100
Fax : (0831) 2405467

REF: VTU/BGM/ACA/2022-23/ 3000

DATE: 3 SEP 2022

NOTIFICATION

Subject: - Academic Calendar of ODD semesters B.E./B.Tech./B.Plan./B.Arch. programs of University regarding...

Reference: Hon'ble Vice-Chancellor's approval dated: 03.09.2022

The academic calendar concerned to **ODD semesters of B.E./B.Tech./B.Plan./B.Arch.** programs of University for academic year 2022-23 are hereby notified as mentioned in the attached sheet;

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges are hereby informed to bring the academic calendar to the notice of all concerned.

Encl: As mentioned

Sd/-

REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The chairperson, Department of Mechanical Engineering /Civil Engineering /Computer Science and Engineering and Business Studies of the University.

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Director I/c. ITI SMU, VTU Belagavi for information and to make arrangements to upload revised Academic Calendar on the VTU web portal.
5. The Director of Physical Education, VTU Belagavi for information
6. PS to Registrar VTU Belagavi
7. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

Reg 03/09/2022 BE

Registrar

Academic Calendar for ODD Semester of UG programs for the year 2022-23

	I semester B.E./B.Tech.	I semester B.Arch./B.Plan	I semester B.Sc.	III semester B.E./ B.Tech.	III Semester B.Arch.	III semester B. Plan	III Semester B.Sc.	V Semester B.E./B.Tech.	V Semester B.Arch./ B.Plan.	VII semester B.E./B.Tech.	VII semester B.Plan.	VII semester B.Arch	IX semester B.Arch
Commencement of ODD Semester	# 10.10.2022	# 10.10.2022	10.10.2022 (Tentative)	11.10.2022	31.10.2022	31.10.2022	10.10.2022	10.10.2022	12.09.2022	21.08.2022	21.08.2022	19.09.2022	01.09.2022
Internship				11.10.2022 To 30.10.2022						21.08.2022 To 17.09.2022	21.08.2022 To 24.09.2022		
Commencement of Classes				31.10.2022	31.10.2022	31.10.2022	10.10.2022	10.10.2022	12.09.2022	19.09.2022	26.09.2022	19.09.2022	01.09.2022
Last Working day of ODD Semester				11.02.2023	11.02.2023	11.02.2023	28.01.2023	27.01.2023	31.12.2022	31.12.2022	07.01.2023	31.12.2022	20.12.2022
Practical Examination				13.02.2023 To 21.02.2023	13.02.2023 To 21.02.2023	13.02.2023 To 21.02.2023	01.02.2023 To 09.02.2023	30.01.2023 To 09.02.2023	03.01.2023 To 13.01.2023	03.01.2023 To 13.01.2023	09.01.2023 To 14.01.2023	03.01.2023 To 13.01.2023	21.12.2022 To 31.12.2022
Theory Examinations				22.02.2023 To 22.03.2023	22.02.2023 To 22.03.2023	22.02.2023 To 22.03.2023	13.02.2023 To 03.03.2023	13.02.2023 To 18.03.2023	16.01.2023 To 15.02.2023	16.01.2023 To 15.02.2023	16.01.2023 To 15.02.2023	16.01.2023 To 15.02.2023	-----
Internship			*	26.03.2023 To 16.04.2023	---	---		---	---		---		---
Internship Viva Voce/ Project viva				---	---	---		---	---	---	---		---
Commencement of EVEN Semester				17.04.2023	17.04.2023	17.04.2023	20.03.2023	20.03.2023	20.03.2023	20.02.2023	20.02.2023	20.02.2023	06.01.2023

Please Note:

- The academic sessions for ODD semesters should commence from the **dates mentioned** above. **# Commencement of Induction Program As per AICTE Academic Calendar 2022-23**
- The commencement date of VII semester B.E./B.Tech/, is postponed from **12.09.2022 to 19.09.2022** to cover 04 weeks of Internship duration. The students of B.E./B.Tech., compulsorily have to complete the Internship in this duration only.
- The commencement date of VII semester B.Plan., is postponed from **12.09.2022 to 26.09.2022** to cover 06 weeks of Internship duration.
- Students joining to VII semester B.E./B.Tech/B.Plan should complete the **Internship** before the commencement of the classes.
- The Institute needs to function for **six days** a week with additional hours **(Saturday is a full working day).** #if required, the college can also plan to have extra classes on Sundays to complete academic activities within the duration mentioned.
- The faculty/staff shall be available to undertake any work assigned by the university.
- Notification regarding the Calendar of Events relating to the conduct of University **Examinations** will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar **may be modified** based on guidelines/directions issued in the future by MHRD/UGC/AICTE/State Government.
- Academic Calendar is also applicable for **Autonomous Colleges.** If any changes are to be effected by Autonomous Colleges in the academic terms and examination schedule, they could do so with the approval of the University.
- The college has to conduct offline classes to cover **80%** of the syllabus of the courses; however, **20%** of the syllabus can be covered in virtual model (Online) mode. **Attendance** of the students for offline and online classes is mandatory and records should be maintained and submitted to the university whenever informed.
- If any clarification/correction, please email to-sbhvtuso@gmail.com

03/09/2022

REGISTRAR

3/9/22

* **Internship for Lateral Entry Students**

DEPARTMENT OF ME

Laboratory Details

SL. No.	Name of the Laboratory	Major Equipment's
1	Workshop Practice EC-004	Files, Hacksaw frames, Bench wise, Welding m/c, Vernier Height Gauge
2	Computer Aided Engineering Drawing	Computers, Software's
3	Mechanical Measurement and Metrology Labrotarty	Sine bar , sin center, LVDT, load cell, profile projector,
4	Machine Shop Laboratory	Lathes, Shaper m/c, Milling m/c, Drilling m/c
5	Foundry and Forging Laboratory	Furnace, sand testing m/c, moisture testing m/c, sand hardness testing m/c
6	Material Testing Laboratory	UTM m/c, Izod and charrpay m/c, Hardness Testing M/cs
7	Fluid Mechanics and Machinery Laboratory	Turbines, Pumps,
8	Energy Conversion Laboratory	Calorimetrs, Visometer, Engines
9	Heat and Mass Transfer	Heat Exchangers, Refrigeration set up, Air condition set up, Condensation set up,
10	Computer Aided Modelling and Analysis Laboratory	Computers, Software
11	Design Laboratory B-006	Governer, Polariscope instrument, Journal bearing , Gyroscope
12	CIM and Automation Laboratory	Computers, Software

Laboratory Details - AIML

SNo.	Name of the Laboratory	Area (Sq. m.)	Major Equipments
1	Computer Lab 1 – E109A AI Lab	70	**30 PCs**: System Configuration: Assemble PC – Intel Core I5- 10th Gen, Azus motherboard prime H410ME, 2.4GHz, 8GB DDR4 RAM, 256GB EVM SSD, USB KBD & USB Optical Mouse, Dell 18.5 LED Monitor 400R SMPS Ubuntu 14.04 NetBeans IDE 8.2 GCC Compiler
2	Computer Lab 2 – E208 ADE Lab	89	**1. 33 PCs**: System Configuration: Assemble PC – Intel Core I5- 10th Gen, Azus motherboard prime H410ME, 2.4GHz, 8GB DDR4 RAM, 256GB EVM SSD, USB KBD & USB Optical Mouse, Dell 18.5 LED Monitor 400R SMPS Window 10 ADE Lab / MES Lab Equipments: 2.1 Signal Generator – 6 Nos 2.2 Power Supply – 6 Nos 2.3 Variable Power Supply – 6 Nos 2.4 Digital IC Trainer Kit – 12 Nos 2.5 Patch Cords – 120 Nos 2.6 Digital IC Tester – 1No 3.Xilinx (Downloaded) 4. Keil V4 Epson Projector
3	Computer Lab 3 – E108 DBMS Lab	59	**30 PCs**: System Configuration: Assemble PC – Intel Core I5- 10th Gen, Azus motherboard prime H410ME, 2.4GHz, 8GB DDR4 RAM, 256GB EVM SSD, USB KBD & USB Optical Mouse, Dell 18.5 LED Monitor 400R SMPS Ubuntu 14.04 NetBeans IDE 8.2 GCC Compiler WZATCO Projector
4	Computer Lab 4 – E109B OOP Lab	110	**33 PCs**: System Configuration: Assemble PC – Intel Core I5- 10th Gen, Azus motherboard prime H410ME, 2.4GHz, 8GB DDR4 RAM, 256GB EVM SSD, USB KBD & USB Optical Mouse, Dell 18.5 LED Monitor 400R SMPS Ubuntu 14.04 NetBeans IDE 8.2 GCC Compiler
-	UPS Battery	-	Vivid Energy 10KVA/120V Techser 7.5KV/120V

MCA Laboratory Details

SNo.	Name of the Laboratory	Major Equipments
1.	**MCA Lab 1** – A321 **UNIX/DBMS/PYTHON/PROJECT/IOT**	30 PCs: System Configaration Assemble PC - Intel(R) Core(TM) i5(10 gen)-10400 CPU @ 2.90GHz, 8.00 GB DDR4 2400MHZ RAM, 256GB EVM SSD 2.5" SATA , USB KBD & USB Optical Mouse, Dell 18.5" 1918H MONITOR + 7.5KVA ONLINE UPS Ubuntu 20.04 LTS
2.	**MCA Lab 2** – A324 **CN/JAVA/PROJECT**	30 PCs: System Configaration: Assemble PC - Intel(R) Core(TM) i5(10 gen)-10400 CPU @ 2.90GHz, 8.00 GB DDR4 2400MHZ RAM, 256GB EVM SSD 2.5" SATA , USB KBD & USB Optical Mouse, Dell 18.5" 1918H MONITOR

Basic Science Laboratory Details

Sl. No	Lab Name	Equipment Details
1	Engineering Physics Lab	1.Two motion traveling microscope 2. Newton's rings microscope 3. Function generator 4. Dual channel power supply 5. Single channel power supply 6. Black body radiator 7. RC Charging discharging unit 8. Sodium vapor lamp 9. Photo diode characteristic kit 10. Fermi Energy kit 11.Ultrasonic interferometer 12. LASER source 13.Screw gauge 14. Torsional pendulum 15. Cathode ray oscilloscope 16.Vernier calipers 17. Spring constant apparatus 18. Optical fibre cable 19.Magnetic field intensity apparatus 20.Digital stop clock 21.Electrical kettle 22.Digital multimeter s etc
2	Engg. Chemistry Lab	1.Digital P^H meter 2.Digital Colorimeter 3.Digital Conductivity meter 4.Digital potentiometer 5.Flame photometer

DEPARTMENT OF CSE

Laboratory Details

SNo.	Name of the Laboratory	Major Equipments
1	Computer Lab 1 – A105 SSOS Lab / OOP Lab	**34 PCs**: Assembled PC – Intel Core I5 2.60GHZ, 8GB DDR4 RAM, 256GB SSD, USB KBD & USB Optical Mouse, Dell 18.5 LED Monitor Ubuntu 20.04 LTS
2	Computer Lab 2 – A103 DBA Lab / CG Lab	**30 PCs:** Intel Core I5-10th Generation, 2.90GHZ, 16GB DDR4 RAM, 2GB Graphics Card, 1TB Hard Disk, USB KBD & USB Optical Mouse, 18.5 LED Monitor. **4 PCs:** Intel Core I5-10th Generation, 2.90GHZ, 8GB DDR4 RAM, 256GB SSD, USB KBD & USB Optical Mouse, 18.5 LED Monitor. Ubuntu 20.04 LTS
3	Computer Lab 3 – A106 AIML Lab / MO Lab	**23 PCs**: 11th GEN Intel Core I5, 3.90GHz, H510 Chipset Gigabyte Motherboard with 8GB DDR4 RAM, 256GB SSD, MK200 Logitech USB KBD & Mouse and Dell 18.5" Monitor. Ubuntu 20.04 LTS **11 PCs**: Intel Core I3 3.60GHZ, 4GB DDR3 RAM, WDC 500GB HDD, USB KBD & USB Optical Mouse, Dell 18.5"Monitor Ubuntu 16.04 LTS
4	Computer Lab 4 – A104 DS Lab / DAA Lab	**37 Pcs**: :11th GEN Intel Core I5, 3.90GHz, H510 Chipset Gigabyte Motherboard with 8GB DDR4 RAM, 256GB SSD, MK200 Logitech USB KBD & Mouse and Dell 18.5" Monitor. Ubuntu 20.04 LTS
5	Computer Lab 5 – A138 Internet Lab	**31 Pcs**:: Intel Core I3 3.60GHZ, 4GB DDR3 RAM, WDC 500GB HDD, USB KBD & USB Optical Mouse, Dell 18.5"Monitor and Hp LaserJet 136NW Ubuntu 16.04 LTS
6	Computer Lab 6 – A136 CN Lab / MAD Lab	**34 PCs:** IIntel Core I5-10th Generation, 2.90GHZ, 16GB DDR4 RAM, 2GB Graphics Card, 1TB Hard Disk, USB KBD & USB Optical Mouse, 18.5 LED Monitor. Ubuntu 20.04 LTS
7	Computer Lab 7 – A133 ADE Lab / M&M Lab	**31 PCs**: Intel Core i3, 4GB RAM, 1 TB HDD, 18.5" LED Display Windows 7 32 bit OS ECLD/ MP Lab Equipments: 2.1. ESA PCI – DIOT Card – 30 Nos 2.2 Signal Generator – 8 Nos 2.3 Power Supply – 12 Nos 2.4 Multimeter – 10 Nos 2.5 Variable Power Supply – 8 Nos 2.6 Digital IC Trainer Kit – 8 Nos 2.7 Patch Cords – 320 Nos 2.8 ApLab Dual Trace Oscilloscope – 8 Nos 2.9 Decade Resistance Box – 4 Nos 2.10 Digital IC Tester – 1No

		2.11. Component organizer – 2 Nos 2.12.Stepper motor – 6 Nos 2.13.Seven Segment – 6 Nos 2.14.Calculator Keyboard Interface – 6 Nos 2.14 Logic controller – 6 Nos 2.16.Dual DIAC – 6 Nos 2.17 ARM-7 LPC Trainer Kit – 10 Nos 2.18 Patch Cards 2.19 Dual DIAC 2.20 CRO – 10 Nos 3. Dot Matrix Printer – 1 No 4. Xilinx (Downloaded) 5. Orcad (Downloaded) 6. TASM / MASM 7. Windows-XP OS
8	Computer Lab 8 – A206 Project Lab	**31 Pcs** : Dell Intel Core i3 3.30 GHZ, 4GB DDR3 RAM, 500GB HDD, USB KBD & USB Optical Mouse, Dell 18.5 LED Monitor Ubuntu 16.04 LTS
9	Computer Lab 9 – A018 CP Lab	**19 Pcs**: I3 processor, Asus H110 Mother board, DDR4 4GB RAM,1 TB SATA Hard disk,18.5" AOC LED Monitor, Keyboard ,Mouse **12 Pcs**: I3 processor, 4GB DDR3 RAM, 500 GB Hard disk, 18.5" AOC LED Monitor, Keyboard, Mouse **10 Pcs**: Intell core I3 processor, H310 mother board, 4GB DDR4 RAM, 1 TB WDC Hard disk with Keyboard, mouse
-	Server Room	**1** Computers – 64GB RAM, 4 TB HDD 1.Mail Server 1.1 Intel Xeon Proessor 1.2 Linux OS 2.IBM Server – 2.1 Intel Xeon E3 2.2 Windows Server 2012 3.Proxy Server 3.1 Intel Core I3 3.2 Linux PF Sence Proxy 4.Laser Printer – 2 Nos 5. DELL i3 Laptop – 1 Nos 6. HP i5 Laptop – 1 Nos 7. Projectors - 6 Nos

Laboratory Details – Dept. of Civil Engineering

SNo.	Name of the Laboratory	Area (Sq. m.)	Major Equipments
1.	Geotechnical Engg Laboratory	161.32	Sieve shaker Motorized, Relative Density Apparatus, Swelling Pressure Test Apparatus,Unconfined Compression Testing Apparatus, Direct shear Apparatus, C.B.R.Testing Machine, Triaxial Testing Machine with Accessories, Permeability Apparatus with Accessories, Consolidation Testing Machine with Dial gauge and loads.
2.	Basic Material Testing Laboratory	100	Universal Testing machine(digital display)100Ton Cap, Rockwell/Brinell Hardness Tester, Impact Testing Machine (Izode\ Charpy), Tile Testing Machine, Torsion Testing Machine Anlog, Motorized sieve shaker.
3.	Basic Surveying practice Laboratory	63.13	Transit Theodalite, Total station with all accessories (Leica), Total station with all accessories (Alldays), Total station with all accessories (South), Dumpy level, Auto Level, Palcom digital plani meter.
4.	Engineering Geology Laboratory	63.13	Magnifying lens (50mm dais), Horse Shoe Magnate, Mineral Specimen, Rock Specimen, Hardness Box, Moh's Scale of Hardness Box, Streak Plates, Structural Geology Models, Banner Flex Sheet, Topo Sheets
5.	Fluid Mechanics Laboratory	86.95	Bernoulli's Theorem verification apparatus, Venturiflume calibration setup, Pressure gauge calibration apparatus (Dead weight type), Collecting tank calibration setup with digital weighing gauge (Gravimetric), Francis Turbine, Venturimeter and Orifice meter calibration setup, Vertical orifice with Tank setup, Notch calibration apparatus with Rectangular ,Triangular and Cippoletti Notches, Weir calibration apparatus with Broad crested and Ogee weir, Friction in pipes apparatus (Major loss), Minor loss apparatus, Single stage Centrifugal pump test setup, Impact of Jet on Vanes apparatus (Hemi-spherical, Flat and Inclined Vane)-with digital Load indicator, Pelton turbine performance test setup, with mechanical loading system, Kaplan turbine performance test setup, with electrical loading system.
6.	Computer Aided Design Lab	79.85	36 Computers, Printers, Projector
7.	Concrete and Highway material Testing Laboratory	169.03	CTM(2000Ton) Capacity Digital, Flexural Testing Machine, Los-Angles Abrasion Apparatus, Aggregate Impact Tests with Counters, Penetration Test Apparatus (2nos), Ductility Testing Machine, Sieve Shaker Motorized 450mm dia,

			VEE-BEE Consistometer, Dorry's abrasion Testing Machine, Tar Viscometer Bitumen Viscosity Device (2units), Vibrating Table, Cube Vibrating Machine, Marshall Stability machine with all Accessories, Bitumen extractor Electricity operated machine, Three-Cell Model Concrete Permeability Test Apparatus with Accessories, (a)Compressor For providing air Sources, Flow Table Motorized, Compacting factor Apparatus, Concrete Mixer, Mortar mixer, Auto Clave (a) Length Comparator, Oven 24"X24"X24", Accelerated Curing Tank, Rebound Hammer, Water Bath, Devel abrasion Testing Machine, J-ring for Self Compacting Concrete, U-Box For Self Compacting Concrete, Flash & Fire point apparatus (2nos).
8.	Environmental Engineering Laboratory	128.46	Auto clave, BOD Incubator, Turbidity Meter, Digital Photo Electric Calorimeter, Jar Testing Apparatus, PH Meter systronics, Digital Conductivity meter, Muffle Furnace(RMF-4), µ Controller based Vis-spectrophotometer with Digital wave length, Hot Air Oven 18x18x18"(RHO-18DF), Flame Photometer, COD Digestion Apparatus, Double Beam UV Spectrometer.

LABORATORY DETAILS (Annexure-I.11) Department wise Laboratory Details

Electronics & Comunication Engineering

Sl. No.	Name of the LAB	Equipments in the LAB as per Scheme and Syllabus
1	Analog electronics lab	CRO Analog/Digital, Signal generator, Regulated Power supply, EPSON Projector, Decade boxes, Multimeter
2	Digital Systeam design Lab	Trainer Kit, IC Tester,
3	Microcontroller lab	Destop PC, Interfacing Kits, EPSON Projector, MSB 430
4	Analog /Advanced Communication lab	CRO Analog/Digital, Signal generator, Regulated Power supply, Fixed Power supply,Microstrip Trainer Kit, Microwave bench setup, EPSON Projector, Decade boxes, Multimeter
5	DSP / HDL Lab	Destop PC, EPSON Projector, Interfacing Kit
6	Embedded syteam design Lab	CRO Analog / Digital, Firing Modules, Regulated Power Supply, Fixed Power supply, Motor & Transformer, Tachometer
7	VLSI / CCN Lab	Destop PC, Cadence Software
8	Project / Research Lab	Computers CRO Power supply Function generator Scanner, Printer, Camera, Web Camera
9	Basic Electrical Lab	KVL / KCL Trainer kit, 3 Volt meter method trainer kit, 2 way and 3 way control of lamp trainer kit, 3 phase autotransformer, messurment of 3 phase power using 2 watt meter trainer kit.
		Total

Visvesvaraya Technological University
Jnana Sangama, Belagavi-590018
VTU-CONSORTIUM

Subscription of E-Resources for the year 2021-22

SL NO	PUBLISHERS	SUBJECT CATEGORY	RESOURCE COVERAGE	NO. OF RESOURCES	CONTACT DETAILS	SUBSCRIPTION PERIOD
1.	**Elsevier** **www.sciencedirect.com**	Engineering + CS + EE + ME + EC and CV	Artificial Intelligence-**22** Computer Graphics and Computer-Aided Design-**19** Computer Networks and Communications-**29** Computer Vision and Pattern Recognition-**10** Hardware and Architecture-**20** Information Systems-**28** Signal Processing-**13** Aerospace Engineering-**5** Biomedical Engineering-**16** Civil and Structural Engineering-**35** Computational Mechanics-**11** Electrical and Electronic Engineering-**33** Mechanical Engineering-**36** Ocean Engineering-**6** Safety, Risk, Reliability and Quality-**13** **(Back Issues from 2010)**	**296 Journals**	**Nikhil Bhalerao** 7428699374 n.bhalerao@elsevier.com	**01-05-2021 to 30-04-2022**
2.	IEEE Proceedings Order Plan (**POP**) **https://ieeexplore.ieee.org** IEEE *Advancing Technology for Humanity*	The core collection of IEEE conference proceedings from approximately 100 of IEEE's most important conferences. Full-text access with a backfile to 2010.	• Aerospace and Defense • Biometrics • Computer Hardware and Software • Cyber Security • Electronics • Internet of Things (IoT) • Medical Devices • Nanotechnology • Optics • Power Engineering • Robotics • Semiconductors • Smart Grid • Telecommunications • Wireless Technology **(Back Issues from 2010)**	**530,000 papers - from 100 core IEEE conference titles in POP**	**Manjunath SR** 9870200104 mrudrappa@ebsco.com	**23-08-2021 to 22-08-2022** After this 1 month compliment.. access up to Sept. 2022
3.	**Springer Nature** **https://link.springer.com/** SPRINGER NATURE	Electrical & Electronics Mechanical Civil Computer Science Engineering (Allied Subject) Chemistry and Material Science Mathematics Physics	Electrical & Electronics - **58** Mechanical - **44** Civil - **13** Computer Science - **93** Engineering (Allied Subject) - **39** Chemistry and Material Science - **162** Mathematics - **167** Physics - **104** **(Back Issues from 1997)**	**690 Journals**	**Varghese P. Thomas** 9686964063 varghese.thomas@springernature.com **Rajaneesh** 9900555516 rajaneesh@springer.com	**01-04-2021 to 31-03-2022**

SL NO	PUBLISHERS	SUBJECT CATEGORY	RESOURCE COVERAGE	NO. OF RESOURCES	CONTACT DETAILS	SUBSCRIPTION PERIOD
4.	**Taylor & Francis** **https://www.tandfonline.com/** Taylor & Francis Taylor & Francis Group	Engineering + CSE + ME + CV + Architecture and Allied Science	Allied Science-**324** Mechanical-**35** Textile -**8** Engineering & Technology-**76** Electrical-**17** Computer Science-**27** Civil & Structural-**31** BioTechnology-**17** Architecture-**19** **(Back Issues from 2010)**	**555 Journals**	**Vinay Srinivas** 9886044775 Vinay.srinivas@tandfindia.com **Onkar Verma** onkar.verma@tandfindia.com Tel: +91-11-43155118	**01-04-2021 to 31-03-2022**
5.	**Emerald** **https://www.emeraldinsight.com/** emerald PUBLISHING	Management	Accounting, Finance & Economics-**9** Business, Management & Strategy-**18** Education-**10** Health & Social Care-**5** HR, Learning & Organization Studies-**17** Information & Knowledge Management-**10** Library Studies-**17** Marketing-**12** Operations, Logistics & Quality-**10** Property Management & Built Environment-**5** Public Policy & Environmental Management-**6** Tourism & Hospitality Management-**1**	**120 Journals**	**S Vinay Kumar** 9916252539 svkumar@emeraldgroup.com	**01-07-2021 to 30-06-2022** After this 3 months compliment.. access up to August 2022
6.	**ProQuest** **https://www.proquest.com/165290** ProQuest	Architecture and all Engineering and it's Allied branches.	Technology Collection includes the Advanced Technology & Aerospace and Materials Science & Engineering Databases **(Back issues from 1962)**	Fulltext: **3900 Journals** Indexed: **7800 Abstract**	**Lakshmikanth A** 9886339117 Lakshmikanth.Aswathanarayan@proquest.com	**01-08-2021 to 31-07-2022**
7.	**Knimbus** **https://new.knimbus.com** knimbus	1. Digital Library Platform 2. Remote Access Solution 3. Mobile App	All subjects 12 K + Resources and following features 1. OA resources: Journals + e-Books + 2. e-Theses + Educational videos 3. 24 X 7 seamless access 4. Admin control for librarians 5. Usage report for individual college can take 6. Secured remote access full text content 7. Mobile compatibility	**E-Books: 10,000+** **E-Journals: 5700+**	**Mohd.Tariq** 9625632330 mohd.tariq@knimbus.com **Venkatesh** 8722937551 venkatesh@knimbus.com	**01-04-2021 to 31-03-2022**

SL NO	PUBLISHERS	SUBJECT CATEGORY	RESOURCE COVERAGE	NO. OF RESOURCES	CONTACT DETAILS	SUBSCRIPTION PERIOD
8.	**Turnitin*** https://www.turnitin.com/ turnitin	Plagiarism Originality Online Check*	End user Licenses: 1. Instructor profile 2. Student's profile	--	Anuab Kumar 981 1464814 akumar@turnitin.com	03-06-2021 to 02-06-2022
9.	**NetAnalytiks** https://sententia.online/ NET ANALYTIKS LANQUILL	LANQUILL (Writing Grammar Tool)	1. Admin control for librarians 2. 24 X 7 seamless access 3. Usage report for individual college can take	--	Laxminaraya na Ullala 9620555571 laks@netanalytiks.com	01-04-2021 to 31-03-2022

Note: *1. *Access given to only 140 PG program Colleges.*
2. Previous years' purchased online e-Books access is continued as perpetual, in the case of McGraw-Hill e-Books subscribed up to 31.05.2023.

VIVEKANANDA
COLLEGE OF ENGINEERING & TECHNOLOGY
[A Unit of Vivekananda Vidyavardhaka Sangha, Puttur ®]
Affiliated to Visvesvaraya Technological University
Approved by AICTE New Delhi & Govt of Karnataka

-
Report
Library
19/09/22

Library Details

PROGRAM		VOLUMES	TITLE	REFERENCE	JOURNALS
UG	ENGINEERING	40387	5377	5396	36
PG	MBA	4995	954	963	12
	MCA	540	129	129	12
TOTAL		**45922**	**6460**	**6488**	**60**

DEPARTMENT WISE BOOKS/JOURNALS

BOOKS			JOURNALS			MAGAZINES	e-Resources
DEPT.	VOLUMES	TITLES	NATIONAL	INTERNATIONAL	TOTAL		
EC	8383	1281	6	-	6	-	1. VTU E-Consortium
CS	9013	1056	6	6	12	-	
ME	7679	863	6	-	6	-	
CV	7623	854	6	-	6	-	
AI	838	167	6	-	6	-	
CD	540	106	-	-	-	-	
IS	2070	325	-	-	-	-	
BS	2940	112	-	-	-	3	
MBA	4995	954	6	6	12	-	
MCA	540	129	6	6	12	-	
GENERAL	1301	613	-	-	-	-	

CD/DVD's - 1741

E-RESOURCES:

E-Books: 25810

E-Journals: 1700

Vivekananda College of Engineering and Technology

Computing facilities available

Sl No	Question	Answer
1	Internet Bandwidth	270 MBPS
2	Number & Configuration of systems	713 & Core i3 and Core i5
3	Total num of system connected by LAN	713
4	Total num of system connected by WAN	0
5	Major Software package available	Oracle 10g MS Visual Studio Pro VLSI (Microwind) Solid Edge Solid works AUTOCAD Microsoft Teams Python Android Studio NetBeans IDE 8.2 Ubuntu
6	Special Purpose Facilites available (Conduct of online Meetings)	Teams software

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
("ವಿ ಟಿ ಯು ಅಧಿನಿಯಮ ೧೯೯೪" ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ)
VISVESVARAYA TECHNOLOGICAL UNIVERSITY
(State University of Government of Karnataka Established as per the VTU Act, 1994)
"JnanaSangama" Belagavi-590018, Karnataka, India

Prof. Dr. B. E. Rangaswamy, Ph.D.
REGISTRAR(I/C)

Phone: (0831) 2498100
Fax : (0831) 2405467

REF: VTU/BGM/ACA/2022-23/ 4197

DATE: 19 NOV 2022

Revised-NOTIFICATION

Subject: - Revised-Academic Calendar of 1st[d] semesters of B.E./B.Tech./B.Arch./B.Plan., programs of University regarding...
Reference: The Hon'ble Vice-Chancellor's approval dated: 18.11.2022

The revised-academic calendar concerned to 1st semester of B.E./B.Tech./B.Arch./B.Plan., programs of University for academic year 2022-23 are hereby notified as mentioned below;

Revised Academic Calendar for I Semester of UG programs for the Academic Year 2022-23 (Tentative)			
Details	**I semester B.E./B.Tech.**	**I semester B.Arch.**	**I semester B.Plan**
**Induction Program	01.12.2022 To 10.12.2022	01.12.2022 To 10.12.2022	01.12.2022 To 10.12.2022
Commencement of I semester Classes	12.12.2022	12.12.2022	12.12.2022
Last Working day of I Semester	31.03.2023	31.03.2023	31.03.2023
Practical Examinations	03.04.2023 To 14.04.2023	03.04.2023 To 14.04.2023	03.04.2023 To 14.04.2023
Theory Examinations	17.04.2023 To 10.05.2023	17.04.2023 To 10.05.2023	17.04.2023 To 10.05.2023
Commencement of II Semester	15.05.2023	15.05.2023	15.05.2023

Please Note:

- The academic sessions for ODD semesters should commence on the **date mentioned** above.

** **Induction Program** shall be conducted for 10 days at the beginning of 1st semester and 11 days at the beginning of the 2nd semester.

During the induction program, college must brief about the new curriculum implemented from the academic year 2022-23.

- The Institute needs to function for **six days** a week with Saturday being half a working day. #if required, the college can also plan to have extra classes on Saturday afternoons and Sundays full day to complete academic activities within the duration mentioned.
- The faculty/staff shall be available to undertake any work assigned by the university.
- Notification regarding the Calendar of Events relating to the conduct of University **Examinations** will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar **may be modified** based on guidelines/directions issued in the future by MHRD/UGC/AICTE/State Government.
- Academic Calendar is also applicable for **Autonomous Colleges.** If any changes are to be effected by Autonomous Colleges in the academic terms and examination schedule, they could do so with the approval of the University.
- AICTE Activity point details circular will be issued by the Registrar's office separately.
- If any clarification/correction, please email to - **sbhvtuso@yahoo.com**

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges, Chairpersons of the University departments are hereby informed to bring the academic calendar to the notice of all concerned.

Sd/-

REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The chairperson, of the Department of Mechanical Engineering /Civil Engineering /Computer Science and Engineering, Electronics & Communication Engineering of the University.

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information.
3. Special Officer QPDS VTU Belagavi for information
4. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
5. The Director I/c. ITI SMU, VTU Belagavi for information and to make arrangements to upload Academic Calendar on the VTU web portal.
6. The Director of Physical Education, VTU Belagavi for information
7. OS for information and make arrangements to send the circular regarding AICTE Activity Points
8. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

19/11/22

REGISTRAR

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
("ವಿ ಟಿ ಯು ಅಧಿನಿಯಮ ೧೯೯೪" ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ)
VISVESVARAYA TECHNOLOGICAL UNIVERSITY
(State University of Government of Karnataka Established as per the VTU Act, 1994)
"JnanaSangama" Belagavi-590018, Karnataka, India

REGISTRAR

Phone : (0831) 2498100
Fax : (0831) 2405467

REF: VTU/BGM/ACA/2022-23/ 3000

DATE: 3 SEP 2022

NOTIFICATION

Subject: - Academic Calendar of ODD semesters B.E./B.Tech./B.Plan./B.Arch. programs of University regarding...

Reference: Hon'ble Vice-Chancellor's approval dated: 03.09.2022

The academic calendar concerned to **ODD semesters of B.E./B.Tech./B.Plan./B.Arch.** programs of University for academic year 2022-23 are hereby notified as mentioned in the attached sheet;

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges are hereby informed to bring the academic calendar to the notice of all concerned.

Encl: As mentioned

Sd/-

REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The chairperson, Department of Mechanical Engineering /Civil Engineering /Computer Science and Engineering and Business Studies of the University.

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Director I/c. ITI SMU, VTU Belagavi for information and to make arrangements to upload revised Academic Calendar on the VTU web portal.
5. The Director of Physical Education, VTU Belagavi for information
6. PS to Registrar VTU Belagavi
7. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

Reg 03/09/2022 BE

Registrar

Academic Calendar for ODD Semester of UG programs for the year 2022-23

	I semester B.E./B.Tech.	I semester B.Arch./B.Plan	I semester B.Sc.	III semester B.E./ B.Tech.	III Semester B.Arch.	III semester B. Plan	III Semester B.Sc.	V Semester B.E./B.Tech.	V Semester B.Arch./ B.Plan.	VII semester B.E./B.Tech.	VII semester B.Plan.	VII semester B.Arch	IX semester B.Arch
Commencement of ODD Semester	# 10.10.2022	# 10.10.2022	10.10.2022 (Tentative)	11.10.2022	31.10.2022	31.10.2022	10.10.2022	10.10.2022	12.09.2022	21.08.2022	21.08.2022	19.09.2022	01.09.2022
Internship				11.10.2022 To 30.10.2022						21.08.2022 To 17.09.2022	21.08.2022 To 24.09.2022		
Commencement of Classes				31.10.2022	31.10.2022	31.10.2022	10.10.2022	10.10.2022	12.09.2022	19.09.2022	26.09.2022	19.09.2022	01.09.2022
Last Working day of ODD Semester				11.02.2023	11.02.2023	11.02.2023	28.01.2023	27.01.2023	31.12.2022	31.12.2022	07.01.2023	31.12.2022	20.12.2022
Practical Examination				13.02.2023 To 21.02.2023	13.02.2023 To 21.02.2023	13.02.2023 To 21.02.2023	01.02.2023 To 09.02.2023	30.01.2023 To 09.02.2023	03.01.2023 To 13.01.2023	03.01.2023 To 13.01.2023	09.01.2023 To 14.01.2023	03.01.2023 To 13.01.2023	21.12.2022 To 31.12.2022
Theory Examinations				22.02.2023 To 22.03.2023	22.02.2023 To 22.03.2023	22.02.2023 To 22.03.2023	13.02.2023 To 03.03.2023	13.02.2023 To 18.03.2023	16.01.2023 To 15.02.2023	16.01.2023 To 15.02.2023	16.01.2023 To 15.02.2023	16.01.2023 To 15.02.2023	-----
Internship			*	26.03.2023 To 16.04.2023	---	---		---	---		---		---
Internship Viva Voce/ Project viva				---	---	---		---	---	---	---		---
Commencement of EVEN Semester				17.04.2023	17.04.2023	17.04.2023	20.03.2023	20.03.2023	20.03.2023	20.02.2023	20.02.2023	20.02.2023	06.01.2023

Please Note:

- The academic sessions for ODD semesters should commence from the **dates mentioned** above. **# Commencement of Induction Program As per AICTE Academic Calendar 2022-23**
- The commencement date of VII semester B.E./B.Tech/, is postponed from **12.09.2022 to 19.09.2022** to cover 04 weeks of Internship duration. The students of B.E./B.Tech., compulsorily have to complete the Internship in this duration only.
- The commencement date of VII semester B.Plan., is postponed from **12.09.2022 to 26.09.2022** to cover 06 weeks of Internship duration.
- Students joining to VII semester B.E./B.Tech/B.Plan should complete the **Internship** before the commencement of the classes.
- The Institute needs to function for **six days** a week with additional hours **(Saturday is a full working day).** #if required, the college can also plan to have extra classes on Sundays to complete academic activities within the duration mentioned.
- The faculty/staff shall be available to undertake any work assigned by the university.
- Notification regarding the Calendar of Events relating to the conduct of University **Examinations** will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar **may be modified** based on guidelines/directions issued in the future by MHRD/UGC/AICTE/State Government.
- Academic Calendar is also applicable for **Autonomous Colleges.** If any changes are to be effected by Autonomous Colleges in the academic terms and examination schedule, they could do so with the approval of the University.
- The college has to conduct offline classes to cover **80%** of the syllabus of the courses; however, **20%** of the syllabus can be covered in virtual model (Online) mode. **Attendance** of the students for offline and online classes is mandatory and records should be maintained and submitted to the university whenever informed.
- If any clarification/correction, please email to-sbhvtuso@gmail.com

03/09/2022

REGISTRAR

3/9/22

* **Internship for Lateral Entry Students**

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
"ಪಟಿಯು ಅಧಿನಿಯಮ ೧೯೯೪"ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ
"ಜ್ಞಾನ ಸಂಗಮ", ಬೆಳಗಾವಿ-೫೯೦೦೧೮, ಕರ್ನಾಟಕ, ಭಾರತ

Visvesvaraya Technological University
(State University of Government of Karnataka Established as per the VTU Act, 1994)
"Jnana Sangama" Belagavi-590018, Karnataka, India
Phone: (0831) 2498100, Fax: (0831) 2405467, Website: vtu.ac.in

Dr. A. S. Deshpande B.E., M.Tech., Ph.D.
Registrar

Phone: (0831) 2498100
Fax: (0831) 2405467

Ref: VTU/BGM/BOS/A9/2021-22 / 3991

Date: 03 DEC 2021

CIRCULAR

Subject: 1st and 2nd -semester scheme(2021) of Teaching and Examinations regarding...

Reference: Hon'ble Vice-Chancellor's approval dated: 03.12.2021

The courses, 21IDT19- Innovation and Design Thinking (offered in 1st semester both for chemistry and physics groups) and 21SFH29- Scientific Foundations of Health (offered in 2nd semester both for chemistry and physics group) are compulsory courses for the students admitting to 1st year B.E./B.Tech. programs.

A slight modification is made in the scheme of teaching and examinations to offer both the courses in 1st as well as 2ndsemester for 50:50 strength of intake. The scheme is attached with this circular for reference and needful. Also, 3-8 semesters scheme template has been attached for stakeholder's information.

All the principals of Engineering Colleges are hereby informed to bring the content of this circular to the notice of the concerned. Please note: corrected scheme of programs is made available @ **https://vtu.ac.in/en/b-e-scheme-syllabus/#menu05**

Sd/-

Registrar

Encl: As mentioned above.

To,

- All the Principals of the Engineering Colleges under the ambit of VTU Belagavi.

Copy to:

1. The Hon'ble Vice-Chancellor through the secretary to VC for information
2. The Registrar(Evaluation) for information and needful
3. The Registrar's Office, VTU, Belagavi, for information.
4. The Special Officer, Academic Section, VTU Belagavi, for information.
5. The Director ITI SMU CNC for information and to upload the circular on the VTU web portal

REGISTRAR

Visvesvaraya Technological University, Belagavi

Scheme of Teaching and Examinations 2021

Outcome-Based Education(OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 – 22)

I Semester (Physics Group) **[Common to all B.E./B.Tech. Programs]**

Sl. No	Course and Course Code		Course Title	Teaching Department (TD)and Paper Setting Board(PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self-Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	BSC	21MAT11	**Calculus & Differential Equations**	TD and PSB: Mathematics	2	2	--		03	50	50	100	3
2	BSC	21PHY12	Engineering Physics	TD and PSB: Physics	2	2	--		03	50	50	100	3
3	ESC	21ELE13	Basic Electrical Engineering	TD and PSB: E and E Engineering	2	2	--		03	50	50	100	3
4	ESC	21CIV14	Elements of Civil Engineering and Mechanics	TD and PSB: Civil Engineering	3	--	--		03	50	50	100	3
5	ESC	21EVN 15	Engineering Visualization	TD: ME, Auto, IP, IEM, Mfg. Engineering PSB: Mechanical Engg	2	--	2		03	50	50	100	3
6	BSC	21PHYL16	Engineering Physics Laboratory	TD and PSB: Physics	--	--	2		03	50	50	100	1
7	ESC	21ELEL17	Basic Electrical Engineering Laboratory	TD and PSB: E and E Engineering	--	--	2		03	50	50	100	1
8	HSMC	21EGH18	Communicative English	TD and PSB: Humanities	1	1	1		02	50	50	100	2
9	AEC	21IDT19/29	Innovation and Design Thinking	Any Engineering Department	1	--	--		01	50	50	100	1
		OR											
		21SFH19/29	Scientific Foundations of Health										
TOTAL					**13**	**07**	**07**		**24**	**450**	**450**	**900**	**20**

Note: BSC: Basic Science Course, **ESC**: Engineering Science Course, **HSMC**: Humanity and Social Science & Management Courses, **AEC** –Ability Enhancement Courses.

L –Lecture**, T –** Tutorial, **P-** Practical/ Drawing, **S –** Self Study Component, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Examination	
Credit definition: 1hour Lecture **(L)** per week = **1 Credit** 2 hours Tutorial **(T)** per week = **1 Credit** 2 hours Practical /Drawing (P) per week = **1 Credit**	(a) **Four-credit** courses are to be designed for **50** hours of Teaching-Learning process. (b) **Three credit** courses are to be designed for **40** hours of Teaching-Learning process. (c) **Two credit** courses are to be designed for **25** hours of Teaching-Learning process. (d) **One-credit** courses are to be designed for **15** hours of Teaching-Learning process.

AICTE Activity Points to be earned by students admitted to BE/B.Tech., /B.Plan day college programme (For more details refer to Chapter 6,AICTE Activity Point Programme, Model Internship Guidelines):

Over and above the academic grades, every Day College regular student admitted to the 4 years Degree programme and every student entering 4 years Degree programme through lateral entry, shall earn 100 and 75 Activity Points respectively for the award of degree through AICTE ActivityPoint Programme. Students transferred from other Universities to the fifth semester are required to earn 50 Activity Points from the year of entry toVTU. The Activity Points earned shall be reflected on the student's eighth semester Grade Card.

The activities can be spread over the years, anytime during the semester weekends and holidays, as per the liking and convenience of the student from the year of entry to the programme. However, the minimum hours' requirement should be fulfilled. Activity Points (non-credit) do not affect SGPA/CGPA and shall not be considered for vertical progression.

In case students fail to earn the prescribed activity Points, an Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of the degree only after the release of the Eighth semester Grade Card.

Summer Internship - I (21INT36): All the students admitted to engineering programmes shall have to undergo a mandatory summer internship of **03 weeks** during the intervening vacation of II and III semesters. Summer Internship shall include Inter / Intra Institutional activities. A University Viva-voce examination (Presentation followed by question-answer session) shall be conducted during III semester and the prescribed credit shall be included in III semester. The internship shall be consideredas a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements. (The faculty coordinator or mentor has to monitor the students' internship progress and interact to guide them for the successful completion of the internship.)

Visvesvaraya Technological University, Belagavi

Scheme of Teaching and Examinations 2021

Outcome-Based Education(OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 – 22)

II Semester (For students who attended I semester under Physics Group) **[Common to all B.E./B.Tech Programs]**

Sl. No	Course and Course Code		Course Title	Teaching Department(TD) and Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self-Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	BSC	21MAT21	Advanced Calculus and Numerical Methods	TD and PSB: Mathematics	2	2	--		03	50	50	100	3
2	BSC	21CHE22	Engineering Chemistry	TD and PSB: Chemistry	2	2	--		03	50	50	100	3
3	ESC	21PSP23	Problem-Solving through Programming	TD and PSB: Computer Science and Engineering	2	2	--		03	50	50	100	3
4	ESC	21ELN24	Basic Electronics & Communication Engineering	TD: ECE/E and I/ TCPSB: ECE	2	2	--		03	50	50	100	3
5	ESC	21EME25	Elements of Mechanical Engineering	TD: ME, Auto, IP,IEM, Mfg . Engineering PSB: Mechanical Engg	2	--	2		03	50	50	100	3
6	BSC	21CHEL26	Engineering Chemistry Laboratory	TD and PSB: Chemistry	--	--	2		03	50	50	100	1
7	ESC	21CPL27	Computer Programming Laboratory	TD and PSB: Computer Science and Engineering	--	--	2		03	50	50	100	1
8	HSMC	21EGH28	Professional Writing Skills in English	TD and PSB: Humanities	1	1	1		02	50	50	100	2
9	AEC	21SFH19/29	Scientific Foundations of Health	Any Department	1	--	--		01	50	50	100	1
		OR											
		21IDT19/29	Innovation and Design Thinking										
				TOTAL	**13**	**09**	**07**		**24**	**450**	**450**	**900**	**20**

Note: BSC: Basic Science Course, **ESC**: Engineering Science Course, **HSMC**: Humanity and Social Science & Management Courses, **AEC** –Ability Enhancement Courses.

L –Lecture**, T –** Tutorial, **P-** Practical/ Drawing, **S –** Self Study Component, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Examination

Credit definition: 1hour Lecture **(L)** per week = **1 Credit** 2 hours Tutorial **(T)** per week = **1 Credit** 2 hours Practical /Drawing (P) per week = **1 Credit**	(a) **Four credit** courses are to be designed for **50** hours of Teaching – Learningprocess. (b) **Three credit** courses are to be designed for **40** hours of Teaching – Learningprocess. (c) **Two credit** courses are to be designed for **25** hours of Teaching – Learning process. (d) **One credit** courses are to be designed for **15** hours of Teaching – Learning process.

AICTE Activity Points to be earned by students admitted to BE/B.Tech.,/B.Plan day college programme (For more details refer to Chapter 6,AICTE Activity Point Programme, Model Internship Guidelines):

Over and above the academic grades, every Day College regular student admitted to the 4 years Degree programme and every student entering 4 years Degree programme through lateral entry, shall earn 100 and 75 Activity Points respectively for the award of degree through AICTE ActivityPoint Programme. Students transferred from other Universities to the fifth semester are required to earn 50 Activity Points from the year of entry toVTU. The Activity Points earned shall be reflected on the student's eighth semester Grade Card.

The activities can be can be spread over the years, anytime during the semester weekends and holidays, as per the liking and convenience of the student from the year of entry to the programme. However, the minimum hours' requirement should be fulfilled. Activity Points (non-credit) do not affect SGPA/CGPA and shall not be considered for vertical progression.

In case students fail to earn the prescribed activity Points, an Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of the degree only after the release of the Eighth semester Grade Card.

Summer Internship - I (21INT36): All the students admitted to engineering programmes shall have to undergo a mandatory summer internship of 03 weeks during the intervening vacation of II and III semesters. Summer Internship shall include Inter / Intra Institutional activities. A University Viva-voce examination (Presentation followed by question-answer session) shall be conducted during III semester and the prescribed credit shall be included in III semester. The internship shall be consideredas a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements. (The faculty coordinator or mentor has to monitor the students' internship progress and interact to guide them for the successful completion of the internship.)

Visvesvaraya Technological University, Belagavi

Scheme of Teaching and Examinations 2021

Outcome-Based Education(OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 – 22)

I Semester (Chemistry Group) **[Common to all B.E./B.Tech. Programmes]**

Sl. No	Course and Course Code		Course Title	Teaching Department (TD)and Paper Setting Board(PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self-Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	BSC	21MAT11	**Calculus & Differential Equations**	TD and PSB: Mathematics	2	2	--		03	50	50	100	3
2	BSC	21CHE12	Engineering Chemistry	TD and PSB: Chemistry	2	2	--		03	50	50	100	3
3	ESC	21PSP13	Problem-Solving through Programming	TD and PSB: Computer Science and Engineering	2	2	--		03	50	50	100	3
4	ESC	21ELN14	Basic Electronics & Communication Engineering	TD: ECE/E and I/ TCPSB: ECE	2	2	--		03	50	50	100	3
5	ESC	21EME15	Elements of Mechanical Engineering	TD: ME, Auto, IP,IEM, Mfg .Engineering PSB: Mechanical Engg	2	--	2		03	50	50	100	3
6	BSC	21CHEL16	Engineering Chemistry Laboratory	TD and PSB: Chemistry	--	--	2		03	50	50	100	1
7	ESC	21CPL17	Computer Programming Laboratory	TD and PSB: Computer Science and Engineering	--	--	2		03	50	50	100	1
8	HSMC	21EGH18	Communicative English	TD and PSB: Humanities	1	1	1		02	50	50	100	2
9	AEC	21IDT19/29	Innovation and Design Thinking	Any Engineering Department	1	--	--		01	50	50	100	1
		OR											
		21SFH19/29	Scientific Foundations of Health										
				TOTAL	**13**	**09**	**07**		**24**	**450**	**450**	**900**	**20**

Note: BSC: Basic Science Course, **ESC**: Engineering Science Course, **HSMC**: Humanity and Social Science & Management Courses, **AEC** –Ability Enhancement Courses.

L –Lecture**, T –** Tutorial, **P-** Practical/ Drawing, **S –** Self Study Component, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Examination	
Credit definition: 1hour Lecture **(L)** per week = **1 Credit** 2 hours Tutorial **(T)** per week = **1 Credit** 2 hours Practical /Drawing (P) per week = **1 Credit**	(a) **Four-credit** courses are to be designed for **50** hours of Teaching-Learning process. (b) **Three credit** courses are to be designed for **40** hours of Teaching-Learning process. (c) **Two credit** courses are to be designed for **25** hours of Teaching-Learning process. (d) **One-credit** courses are to be designed for **15** hours of Teaching-Learning process.

AICTE Activity Points to be earned by students admitted to BE/B.Tech., /B.Plan day college programme (For more details refer to Chapter 6,AICTE Activity Point Programme, Model Internship Guidelines):

Over and above the academic grades, every Day College regular student admitted to the 4 years Degree programme and every student entering 4 years Degree programme through lateral entry, shall earn 100 and 75 Activity Points respectively for the award of degree through AICTE ActivityPoint Programme. Students transferred from other Universities to the fifth semester are required to earn 50 Activity Points from the year of entry toVTU. The Activity Points earned shall be reflected on the student's eighth semester Grade Card.

The activities can be spread over the years, anytime during the semester weekends and holidays, as per the liking and convenience of the student from the year of entry to the programme. However, the minimum hours' requirement should be fulfilled. Activity Points (non-credit) do not affect SGPA/CGPA and shall not be considered for vertical progression.

In case students fail to earn the prescribed activity Points, an Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of the degree only after the release of the Eighth semester Grade Card.

Summer Internship - I (21INT36): All the students admitted to engineering programmes shall have to undergo a mandatory summer internship of **03 weeks** during the intervening vacation of II and III semesters. Summer Internship shall include Inter / Intra Institutional activities. A University Viva-voce examination (Presentation followed by question-answer session) shall be conducted during III semester and the prescribed credit shall be included in III semester. The internship shall be consideredas a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements. (The faculty coordinator or mentor has to monitor the students' internship progress and interact to guide them for the successful completion of the internship.)

Visvesvaraya Technological University, Belagavi

Scheme of Teaching and Examinations 2021

Outcome-Based Education(OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 – 22)

II Semester (For students who attended 1st semester under Chemistry Group) **[Common to all B.E./B.Tech Programs]**

Sl. No	Course and Course Code		Course Title	Teaching Department(TD) and Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self-Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	BSC	21MAT21	Advanced Calculus and Numerical Methods	TD and PSB: Mathematics	2	2	--		03	50	50	100	3
2	BSC	21PHY22	Engineering Physics	TD and PSB: Physics	2	2	--		03	50	50	100	3
3	ESC	21ELE23	Basic Electrical Engineering	TD and PSB: E and E Engineering	2	2	--	--	03	50	50	100	3
4	ESC	21CIV24	Elements of Civil Engineering and Mechanics	TD and PSB: Civil Engineering	3	--	--		03	50	50	100	3
5	ESC	21EVN 25	Engineering Visualization	TD: ME, Auto, IP,IEM, Mfg. Engineering PSB: Mechanical Engg	2	--	2		03	50	50	100	3
6	BSC	21PHYL26	Engineering Physics Laboratory	TD and PSB: Physics	--	--	2		03	50	50	100	1
7	ESC	21ELEL27	Basic Electrical Engineering Laboratory	TD and PSB: E and E Engineering	--	--	2		03	50	50	100	1
8	HSMC	21EGH28	Professional Writing Skills in English	TD and PSB: Humanities	1	1	1		02	50	50	100	2
9	AEC	21SFH19/29	Scientific Foundations of Health	Any Department	1	--	--		01	50	50	100	1
		OR											
		21IDT19/29	Innovation and Design Thinking										
				TOTAL	**13**	**07**	**07**		**24**	**450**	**450**	**900**	**20**

Note: BSC: Basic Science Course, **ESC**: Engineering Science Course, **HSMC**: Humanity and Social Science & Management Courses, **AEC** –Ability Enhancement Courses.

L –Lecture**, T –** Tutorial, **P-** Practical/ Drawing, **S –** Self Study Component, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Examination

Credit definition: 1hour Lecture **(L)** per week = **1 Credit** 2 hours Tutorial **(T)** per week = **1 Credit** 2 hours Practical /Drawing (P) per week = **1 Credit**	(a) **Four credit** courses are to be designed for **50** hours of Teaching – Learningprocess. (b) **Three credit** courses are to be designed for **40** hours of Teaching – Learningprocess. (c) **Two credit** courses are to be designed for **25** hours of Teaching – Learning process. (d) **One credit** courses are to be designed for **15** hours of Teaching – Learning process.

AICTE Activity Points to be earned by students admitted to BE/B.Tech.,/B.Plan day college programme (For more details refer to Chapter 6,AICTE Activity Point Programme, Model Internship Guidelines):

Over and above the academic grades, every Day College regular student admitted to the 4 years Degree programme and every student entering 4 years Degree programme through lateral entry, shall earn 100 and 75 Activity Points respectively for the award of degree through AICTE Activity Point Programme. Students transferred from other Universities to the fifth semester are required to earn 50 Activity Points from the year of entry to VTU. The Activity Points earned shall be reflected on the student's eighth semester Grade Card.

The activities can be can be spread over the years, anytime during the semester weekends and holidays, as per the liking and convenience of the student from the year of entry to the programme. However, the minimum hours' requirement should be fulfilled. Activity Points (non-credit) do not affect SGPA/CGPA and shall not be considered for vertical progression.

In case students fail to earn the prescribed activity Points, an Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of the degree only after the release of the Eighth semester Grade Card.

Summer Internship - I (21INT36): All the students admitted to engineering programmes shall have to undergo a mandatory summer internship of 03 weeks during the intervening vacation of II and III semesters. Summer Internship shall include Inter / Intra Institutional activities. A University Viva-voce examination (Presentation followed by question-answer session) shall be conducted during III semester and the prescribed credit shall be included in III semester. The internship shall be consideredas a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements. (The faculty coordinator or mentor has to monitor the students' internship progress and interact to guide them for the successful completion of the internship.)

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Artificial Intelligence and Machine Learning

Scheme of Teaching and Examinations2021

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

III SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21MAT31	Transform Calculus, Fourier Series and Numerical Techniques	Maths	3	0	0		03	50	50	100	3
2	IPCC 21CS32	Data Structures and its Applications	Any CS Board Department	3	0	2		03	50	50	100	4
3	IPCC 21CS33	Analog and Digital Electronics		3	0	2		03	50	50	100	4
4	PCC 21CS34	Computer Organization and Architecture		3	0	0		03	50	50	100	3
5	PCC 21CSL35	Object Oriented Programming with JAVA Laboratory		0	0	2		03	50	50	100	1
6	UHV 21UH36	Social Connect and Responsibility	Any Department	0	0	1		01	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	TD and PSB: HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India and Professional Ethics										
8	AEC 21CS38X/21 CSL38X	Ability Enhancement Course - III	TD: Concerned department PSB: Concerned Board	If offered as Theory Course: 1	0	0		01	50	50	100	1
				If offered as lab. course: 0	0	2		02				
								Total	**400**	**400**	**800**	**18**
9	**Scheduled activities for III to VIII semesters**	NMDC 21NS83	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out from (for 5 semesters) between III semester to VIII semester. SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the colander prepared for the NSS, PE and Yoga activities.								
		NMDC 21PE83	Physical Education (PE) (Sports and Athletics)	PE								
		NMDC 21YO83	Yoga	Yoga								

Course prescribed to lateral entry Diploma holders admitted to III semester B.E./B.Tech programs

1	NCMC 21MATDIP31	Additional Mathematics - I	Maths	02	02	--	--	---	100	---	100	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course.
L –Lecture, **T –** Tutorial, P- Practical/ Drawing, **S –** Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination. **TD-**Teaching Department, **PSB**: Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and **21KBK37/47** Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical's of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

21INT49 Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internship of 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and has no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Ability Enhancement Course - III			
21CSL381	Mastering Office	21CS383	
21CS382	Programming in C++	21CS384	

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Artificial Intelligence and Machine Learning

Scheme of Teaching and Examinations 2021

Outcome-Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

IV SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21CS41	Mathematical Foundations for Computing	Maths	2	2	0		03	50	50	100	3
2	IPCC 21CS42	Design and Analysis of Algorithms	Any CS Board Department	3	0	2		03	50	50	100	4
3	IPCC 21CS43	Microcontroller and Embedded Systems		3	0	2		03	50	50	100	4
4	PCC 21CS44	Operating Systems		2	2	0		03	50	50	100	3
5	AEC 21BE45	Biology For Engineers	BT, CHE, PHY	2	0	0		02	50	50	100	2
6	PCC 21CSL46	Python Programming Laboratory	Any CS Board Department	0	0	2		03	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India & Professional Ethics										
8	AEC 21CS48X/21CSL48X	Ability Enhancement Course- IV	TD and PSB: Concerned department	If offered as theory Course: 1	0	0		01	50	50	100	1
				If offered as lab. course: 0	0	2		02				
9	UHV 21UH49	Universal Human Values	Any Department	1	0	0		01	50	50	100	1
10	INT 21INT49	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period of II and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.				3	100	--	100	2
								Total	**550**	**450**	**1000**	**22**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

1	NCMC 21MATDIP41	Additional Mathematics - II	Maths	02	02	--	--	--	100	--	100	0

Note: BSC: Basic Science Course, IPCC: Integrated Professional Core Course, PCC: Professional Core Course, AEC –Ability Enhancement Courses, HSMC: Humanity and Social Science and Management Courses, UHV- Universal Human Value Courses.

L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical's of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from practical part of IPCC shall be included in the SEE question paper. For more details the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

Non – credit mandatory course (NCMC):

Additional Mathematics - II:

(1) Lateral entry Diploma holders admitted to III semester of B.E./B.Tech., shall attend the classes during the IV semester to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfil the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and has no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the course Additional Mathematics II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics II shall be indicated as Unsatisfactory.

Ability Enhancement Course - IV

21CSL481	Web Programming	21CSL483	R Programming
21CS482	Unix Shell Programming	21CS484	

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68 Innovation/ Entrepreneurship/ Societal based Internship.

(1) All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be considered under F (fail) grade and shall have to complete during subsequently after satisfying the internship requirements.

(2) Innovation/ Entrepreneurship Internship shall be carried out at industry, State and Central Government /Non-government organizations (NGOs), micro, small and medium enterprise (MSME), Innovation centers or Incubation centers. Innovation need not be a single major breakthrough; it can also be a series of small or incremental changes. Innovation of any kind can also happen outside of the business world.

Entrepreneurship internships offers a chance to gain hands on experience in the world of entrepreneurship and helps to learn what it takes to run a small entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business endeavours. Start-ups and small companies are a preferred place to learn the business tack ticks for future entrepreneurs as learning how a small business operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open the minds to creativity and innovation. Entrepreneurship internship can be from several sectors, including technology, small and medium-sized, and the service sector.

(3) Societal or social internship.

Urbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of many things that urban population enjoy. Rural internship, is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for better living.

As proposed under the AICTE rural internship programme, activities under Societal or social internship, particularly in rural areas, shall be considered for 40 points under AICTE activity point programme.

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V SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21CS51	Automata Theory and compiler Design	Any CS Board Department	3	0	0		03	50	50	100	3
2	IPCC 21CS52	Computer Networks		3	0	2		03	50	50	100	4
3	PCC 21CS53	Database Management Systems		3	0	0		03	50	50	100	3
4	PCC 21AI54	Principles of Artificial Intelligence		3	0	0		03	50	50	100	3
5	PCC 21CSL55	Database Management Systems Laboratory with Mini Project		0	0	2		03	50	50	100	1
6	AEC 21XX56	Research Methodology & Intellectual Property Rights	TD: Any Department PSB: As identified by university	2	0	0		02	50	50	100	2
7	HSMC 21CIV57	Environmental Studies	TD: Civil/ Environmental /Chemistry/ Biotech. PSB: Civil Engg	1	0	0		1	50	50	100	1
8	AEC 21CS58X/21 CSL58X	Ability Enhancement Course-V	Concerned Board	If offered as Theory courses				01	50	50	100	1
				1	0	0						
				If offered as lab. courses				02				
				0	0	2						
								Total	**400**	**400**	**800**	**18**

Ability Enhancement Course - IV

21CSL581	Angular JS and Node JS	21CS583	
21CS582	C# and .Net Framework	21CS584	

Note: BSC: Basic Science Course, PCC: Professional Core Course, IPCC: Integrated Professional Core Course, AEC –Ability Enhancement Course INT – Internship, HSMC: Humanity and Social Science & Management Courses.
L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Integrated Professional Core Course (IPCC): refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). Theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by CIE only and there shall be no SEE. For more details the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

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VI SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	HSMC 21CS61	Software Engineering and Project Management	Any CS Board Department	2	2	0		03	50	50	100	3
2	IPCC 21AD62	Data Science and its Applications		3	0	2		03	50	50	100	4
3	PCC 21AI63	Machine Learning		3	0	0		03	50	50	100	3
4	PEC 21XX64x	Professional Elective Course-I		3	0	0		03	50	50	100	3
5	OEC 21XX65x	Open Elective Course-I	Concerned Department	3	0	0		03	50	50	100	3
6	PCC 21AIL66	Machine Learning Laboratory	Any CS Board Department	0	0	2		03	50	50	100	1
7	MP 21AIMP67	Mini Project		Two contact hours /week for interaction between the faculty and students.				--	100	--	100	2
8	INT 21INT68	Innovation/Entrepreneurship /Societal Internship	Completed during the intervening period of IV and V semesters.					--	100	--	100	3
								Total	**500**	**300**	**800**	**22**

Professional Elective - I

21AI641	Business Intelligence	21AI643	Natural Language Processing
21CS642	Advanced JAVA Programming	21AI644	Computer Graphics and Fundamentals of Image Processing

Open Electives – I offered by the Department to other Department students

21CS651	Introduction to Data Structures	21CS653	Introduction to Cyber Security
21CS652	Introduction to Database Management Systems	21CS654	Programming in JAVA

Note: HSMC: Humanity and Social Science & Management Courses, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **PEC:** Professional Elective Courses, OEC–Open Elective Course, **MP** –Mini Project, INT –Internship.
L –Lecture, T – Tutorial, P - Practical / Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by CIE only and there shall be no SEE. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech) 2021-22 may be referred.

Professional Elective Courses (PEC):
A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course out of five courses. The minimum students' strength for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the programme is less than 10.

Open Elective Courses:
Students belonging to a particular stream of Engineering and Technology are not entitled for the open electives offered by their parent Department. However, they can opt an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor.
Selection of an open elective shall **not be allowed** if,

(i) The candidate has studied the same course during the previous semesters of the program.
(ii) The syllabus content of open electives is similar to that of the Departmental core courses or professional electives.
(iii) A similar course, under any category, is prescribed in the higher semesters of the program.

In case, any college is desirous of offering a course (not included in the Open Elective List of the University) from streams such as Law, Business (MBA), Medicine, Arts, Commerce, etc., can seek permission, at least one month before the commencement of the semester, from the University by

submitting a copy of the syllabus along with the details of expertise available to teach the same in the college.
The minimum students' strength for offering open electives is 10. However, this conditional shall not be applicable to cases where the admission to the programme is less than 10.

Mini-project work: Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications.
Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.
CIE procedure for Mini-project:
(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two faculty members of the Department, one of them being the Guide. The CIE marks awarded for the Mini-project work shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the project.
The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
No SEE component for Mini-Project.

VII semester Classwork and Research Internship /Industry Internship (21INT82)

Swapping Facility
Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate research internship/ industry internship after the VI semester**.**
(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the program.
Elucidation:
At the beginning of IV year of the programme i.e., after VI semester, VII semester classwork and VIII semester Research Internship /Industrial Internship shall be permitted to be operated simultaneously by the University so that students have ample opportunity for internship. In other words, a good percentage of the class shall attend VII semester classwork and similar percentage of others shall attend to Research Internship or Industrial Internship.
Research/Industrial Internship shall be carried out at an Industry, NGO, MSME, Innovation centre, Incubation centre, Start-up, Centers of Excellence (CoE), Study Centre established in the parent institute and /or at reputed research organizations / institutes. The internship can also be rural internship.
The mandatory Research internship /Industry internship is for 24 weeks. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during the subsequent University examination after satisfying the internship requirements.

INT21INT82 Research Internship/ Industry Internship/Rural Internship
Research internship: A research internship is intended to offer the flavour of current research going on in the research field. It helps students get familiarized with the field and imparts the skill required for carrying out research.
Industry internship: Is an extended period of work experience undertaken by students to supplement their degree for professional development. It also helps them learn to overcome unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with contingencies helps students recognize, appreciate, and adapt to organizational realities by tempering their knowledge with practical constraints.
Rural internship: A long-term goal, as proposed under the AICTE rural internship programme, shall be counted as rural internship activity.
The student can take up Interdisciplinary Research Internship or Industry Internship.
The faculty coordinator or mentor has to monitor the students' internship progress and interact with them to guide for the successful completion of the internship.
The students are permitted to carry out the internship anywhere in India or abroad. University shall not bear any expenses incurred in respect of internship.

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Swappable VII and VIII SEMESTER

VII SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	PCC 21AI71	Advanced AI and ML	Any CS Board Department	3	0	0		3	50	50	100	3
2	PCC 21CS72	Cloud Computing		2	0	0		3	50	50	100	2
3	PEC 21XX73X	Professional elective Course-II		3	0	0		3	50	50	100	3
4	PEC 21XX74X	Professional elective Course-III		3	0	0		3	50	50	100	3
5	OEC 21XX75X	Open elective Course-II	Concerned Department	3	0	0		3	50	50	100	3
6	Project 21AIP76	Project work		Two contact hours /week for interaction between the faculty and students.				3	100	100	200	10
								Total	**350**	**350**	**700**	**24**

VIII SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	Seminar 21AI81		Technical Seminar		One contact hour /week for interaction between the faculty and students.				--	100	--	100	01
2	INT 21INT82		Research Internship/ Industry Internship		Two contact hours /week for interaction between the faculty and students.				03 (Batch wise)	100	100	200	15
3	NCMC	21NS83	National Service Scheme (NSS)	NSS	Completed during the intervening period of III semester to VIII semester.				--	50	50	100	0
		21PE83	Physical Education (PE) (Sports and Athletics)	PE									
		21YO83	Yoga	Yoga									
									Total	**250**	**150**	**400**	**16**

Professional Elective - II

21AI731	Social Network Analysis	21CS734	Blockchain Technology
21CS732	Digital Image Processing	21CS735	Internet of Things
21AI733	Fullstack Development		

Professional Elective - III

21AI741	Augmented Reality	21CS744	Robotic Process Automation Design and Development
21CS742	Multiagent Systems	21CS745	NoSQL Data Base
21AI743	Predictive Analytics		

Open Electives - II offered by the Department to other Department students			
21CS751	Programming in Python	21CS754	Introduction to Data Science
21CS752	Introduction to AI and ML	21CS755	
21CS753	Introduction to Big Data		

Note: PCC: Professional Core Course, **PEC:** Professional Elective Courses, **OEC**–Open Elective Course, **AEC** –Ability Enhancement Courses.
L –Lecture, T – Tutorial, P- Practical / Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Note: VII and VIII semesters of IV year of the programme

(1) Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate research internship/ industry internship after the VI semester**.**

(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the programme.

PROJECT WORK (21XXP76): The objective of the Project work is

(i) To encourage independent learning and the innovative attitude of the students.
(ii) To develop interactive attitude, communication skills, organization, time management, and presentation skills.
(iii) To impart flexibility and adaptability.
(iv) To inspire team working.
(v) To expand intellectual capacity, credibility, judgment and intuition.
(vi) To adhere to punctuality, setting and meeting deadlines.
(vii) To instil responsibilities to oneself and others.
(viii) To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

CIE procedure for Project Work:

(1) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(2) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable. The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE procedure for Project Work: SEE for project work will be conducted by the two examiners appointed by the University. The SEE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25.

TECHNICAL SEMINAR (21XXS81): The objective of the seminar is to inculcate self-learning, present the seminar topic confidently, enhance communication skill, involve in group discussion for exchange of ideas. Each student, under the guidance of a Faculty, shall choose, preferably, a recent topic of his/her interest relevant to the programme of Specialization.

(i) Carry out literature survey, systematically organize the content.
(ii) Prepare the report with own sentences, avoiding a cut and paste act.
(iii) Type the matter to acquaint with the use of Micro-soft equation and drawing tools or any such facilities.
(iv) Present the seminar topic orally and/or through PowerPoint slides.
(v) Answer the queries and involve in debate/discussion.
(**vi)** Submit a typed report with a list of references.

The participants shall take part in the discussion to foster a friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Evaluation Procedure:

The CIE marks for the seminar shall be awarded (based on the relevance of the topic, presentation skill, participation in the question and answer session, and quality of report) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three teachers from the department with the senior-most acting as the Chairman.

Marks distribution for CIE of the course:

Seminar Report:50 marks
Presentation skill:25 marks
Question and Answer: 25 marks. ■ No SEE component for Technical Seminar

Non – credit mandatory courses (NCMC):

National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they has to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequently to earn the qualifying CIE marks subject to the maximum programme period.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

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III SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21MAT31	Transform Calculus, Fourier Series and Numerical Techniques (Common to all)	TD- Maths PSB-Maths	2	2	0	0	03	50	50	100	3
2	IPCC 21CV32	Geodetic Engineering	TD: Civil Engg PSB: Civil Engg	2	2	2	0	03	50	50	100	4
3	IPCC 21CV33	Strength of Materials	TD: Civil Engg PSB: Civil Engg	2	2	2	0	03	50	50	100	4
4	**PCC 21CV34**	**Earth Resources and Engineering**	**TD: Geology PSB: Geology**	**3**	**0**	**0**	**0**	**03**	**50**	**50**	**100**	**3**
5	PCC 21CVL35	Computer Aided Building Planning and Drawing	TD: Civil Engg PSB: Civil Engg	0	0	2	0	03	50	50	100	1
6	UHV 21UH36	Social Connect and Responsibility	Any Department	0	0	2	0	01	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	TD and PSB HSMC	0	2	0	0	01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India and Professional Ethics										
8	AEC 21CV38X	Ability Enhancement Course - III	TD: Concerned department PSB: Concerned Board	If offered as Theory Course: 0	2	0		01	50	50	100	1
				If offered as lab. course: 0	0	2		02				
								Total	**400**	**400**	**800**	**18**
9	**Scheduled activities for III to VIII semesters**	NCMC 21NS83	National Service Scheme (NSS)	NSS	All students have to register for any one of the courses namely National Service Scheme, Physical Education (PE)(Sports and Athletics),and Yoga with the concerned coordinator of the course during the first week of III semester.The activities shall be carried out between III semester to VIII semester (for 5 semesters). SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities.									
		NCMC 21PE83	Physical Education (PE)(Sports and Athletics)	PE								
		NCMC 21YO83	Yoga	Yoga								

Course prescribed to lateral entry Diploma holders admitted to III semester B.E./B.Tech programs

1	NCMC 21MATDIP31	Additional Mathematics - I	Maths	02	02	--	--	---	100	---	100	0

Note:BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course,**INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course.

L –Lecture, **T –** Tutorial, P- Practical/ Drawing, **S –** Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD-**Teaching Department, **PSB**: Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and **21KBK37/47** Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the

SEE question paper.For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

21INT49Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internshipof 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card.The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A)Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the coursesAdditional Mathematics I and IIshall be indicated as satisfactory in the grade card. Non-completion of the coursesAdditional Mathematics I and IIshall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE, nd 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Ability Enhancement Course - III

21CV381	Problem Solving using Python	21CV384	Infrastructure Finance
21CV382	Microsoft Excel and Visual Basic for Application	21CV385	Fire Safety in Buildings
21CV383	Personality Development and Soft Skills		

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IV SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC **21MAT41**	Complex Analysis, Probability and Statistical Methods.	TD, PSB-Maths	2	2	0	0	03	50	50	100	3
2	IPCC 21CV42	Fluid Mechanics and Hydraulics	TD: Civil Engg PSB: Civil Engg	2	2	2	0	03	50	50	100	4
3	IPCC 21CV43	Public Health Engineering	TD: Civil Engg PSB: Civil Engg	2	2	2	0	03	50	50	100	4
4	PCC 21CV44	Analysis of Structures	TD: Civil Engg PSB: Civil Engg	2	2	0	0	03	50	50	100	3
5	AEC 21BE45	Biology for Engineers	BT, CHE, PHY	1	2	0	0	02	50	50	100	2
6	PCC 21CVL46	Earth Resources and Engineering Lab	TD: Geology PSB: Geology	0	0	2	0	03	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	HSMC	0	2	0	0	01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India & Professional Ethics										
8	AEC 21CV48X	Ability Enhancement Course- IV	TD and PSB: Concerned department	If offered as theory Course: 0	2	0		01	50	50	100	1
				If offered as lab. course: 0	0	2		02				
9	UHV 21UH49	UniversalHumanValues	Any Department	0	2	0		01	50	50	100	1
10	INT 21INT49	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period ofII and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.				3	100	--	100	2
								Total	**550**	**450**	**1000**	**22**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

1	NCMC 21MATDIP41	Additional Mathematics - II	Maths	02	02	--	--	--	100	--	100	0

Note: BSC: Basic Science Course, IPCC: Integrated Professional Core Course, PCC: Professional Core Course, AEC –Ability Enhancement Courses, HSMC: Humanity and Social Science and Management Courses, UHV- Universal Human Value Courses.

L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCCshall be included in the SEE question paper.For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

Non – credit mandatory course (NCMC):

Additional Mathematics - II:

(1) Lateral entry Diploma holders admitted to III semester of B.E./B.Tech., shall attend the classes during the IV semester to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the course Additional Mathematics IIshall be indicated as satisfactory in the grade card. Non-completion of the courses. Additional Mathematics IIshall be indicated as Unsatisfactory.

Ability Enhancement Course - IV			
21CV481	Data Cleaning and Preparation with Python Pandas	21CV484	Project Finance
21CV482	GIS with Quantum GIS	21CV485	Green Buildings
21CV483	Technical Writing Skills		

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68Innovation/ Entrepreneurship/ Societal Internship.

(1) All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card.The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be considered under F (fail) grade and shall have to complete it subsequently after satisfying the internship requirements.

(2)Innovation/ Entrepreneurship Internshipshall be carried out at industry, State and Central Government /Non-government organizations (NGOs), micro, small and medium enterprises (MSME), Innovation centres, or Incubation centers etc. Innovation need not be a single major breakthrough; it can also be a series of small or incremental changes. Innovation of any kind can also happen outside of the business world.

Entrepreneurship internships offer a chance to gain hands-on experience in the world of entrepreneurship and help to learn what it takes to run a small entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business endeavors.Start-ups and small companies are a preferred places to learn the business tactics for future entrepreneurs as earning how a small business operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open minds to creativity and innovation.Entrepreneurship internships can be from several sectors, including technology, small and medium-sized sector, and the service sector.

(3) **Societal or Social internship.**Urbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of many things that urban population enjoys. The rural internship is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for better living.

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V SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21CV51	Hydrology and Water Resources Engineering	TD: Civil Engg PSB: Civil Engg	3	0	0		03	50	50	100	3
2	IPCC 21CV52	Transportation Engineering	TD: Civil Engg PSB: Civil Engg	2	2	2		03	50	50	100	4
3	PCC 21CV53	Design of RC Structural Elements	TD: Civil Engg PSB: Civil Engg	2	2	0		03	50	50	100	3
4	PCC 21CV54	Geotechnical Engineering	TD: Civil Engg PSB: Civil Engg	2	2	0		03	50	50	100	3
5	PCC 21CVL55	Geotechnical Engineering Lab	TD: Civil Engg PSB: Civil Engg	0	0	2		03	50	50	100	1
6	AEC 21CV56	Research Methodology & Intellectual Property Rights	TD: Any Department PSB: As identified by University	1	2	0		02	50	50	100	2
7	HSMC 21CIV57	Environmental Studies	TD: Civil/ Environmental /Chemistry/ Biotech. PSB: Civil Engg	0	2	0		1	50	50	100	1
8	AEC 21CV58X	Ability Enhancement Course-V	Concerned Board	If offered as Theory courses: 0	2	0		01	50	50	100	1
				If offered as lab. courses: 0	0	2		02				
								Total	**400**	**400**	**800**	**18**

Ability Enhancement Course - V

21CV581	Data Analysis with Python	21CV584	Quality Control and Quality Assurance
21CV582	Software Applications	21CV585	Offshore Structures
21CV583	Gender Sensitization		

Note: BSC: Basic Science Course, PCC: Professional Core Course, IPCC: Integrated Professional Core Course, AEC –Ability Enhancement Course INT – Internship, HSMC: Humanity and Social Science & Management Courses.

L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Integrated Professional Core Course (IPCC): refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by CIE only and there shall be no SEE. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

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VI SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	HSMC 21CV61	Construction Management and Entrepreneurship	TD: Civil Engg PSB: Civil Engg	3	0	0		03	50	50	100	3
2	IPCC 21CV62	Concrete Technology	TD: Civil Engg PSB: Civil Engg	2	2	2		03	50	50	100	4
3	PCC 21CV63	Design of Steel structure	TD: Civil Engg PSB: Civil Engg	2	2	0		03	50	50	100	3
4	PEC 21CV64x	Professional Elective Course-I	TD: Civil Engg PSB: Civil Engg	3	0	0		03	50	50	100	3
5	OEC 21CV65x	Open Elective Course-I	Concerned Department	3	0	0		03	50	50	100	3
6	PCC 21CVL66	Computer Aided Detailing of Structure	TD: Civil Engg PSB: Civil Engg	0	0	2		03	50	50	100	1
7	MP 21CVMP67	Mini Project - Extensive survey project	TD: Civil Engg PSB: Civil Engg	Two contact hours /week for interaction between the faculty and students.				--	100	--	100	2
8	INT 21INT68	Innovation/Entrepreneurship /Societal Internship	Completed during the intervening period of IV and V semesters.					--	100	--	100	3
								Total	**500**	**300**	**800**	**22**

Professional Elective - I

21CV641	Design of Prestressed Concrete Structures	21CV644	Design Concept in Building Services
21CV642	Applied Geotechnical Engineering	21CV645	Ground Water Hydraulics
21CV643	Railways, Harbours, Tunnelling and Airports	21CV646	Alternative Building Materials

Open Electives – I offered by the Department to other Department students

21CV651	Remote Sensing and GIS	21CV653	Occupational Health and Safety
21CV652	Traffic Engineering	21CV654	Conservation of Natural Resources

Note:HSMC: Humanity and Social Science & Management Courses, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **PEC:** Professional Elective Courses, O**EC**–Open Elective Course, **MP** –Mini Project, INT –Internship.
L –Lecture, **T** – Tutorial, **P** - Practical / Drawing, **S** – Self Study Component, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Examination.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by CIE only and there shall be no SEE. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech) 2021-22 may be referred.

Professional Elective Courses(PEC):
A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10.

Open Elective Courses:
Students belonging to a particular stream of Engineering and Technology are not entitled to the open electives offered by their parent Department. However, they can opt for an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor.
Selection of an open elective shall **not be allowed** if,

(i) The candidate has studied the same course during the previous semesters of the program.

(ii) The syllabus content of open electives is similar to that of the Departmental core courses or professional electives.

(iii) A similar course, under any category, is prescribed in the higher semesters of the program.

In case, any college is desirous of offering a course (not included in the Open Elective List of the University) from streams such as Law, Business (MBA), Medicine, Arts, Commerce, etc., can seek permission, at least one month before the commencement of the semester, from the University by submitting a copy of the syllabus along with the details of expertise available to teach the same in the college.

The minimum students' strength for offering open electives is 10. However, this conditional shall not be applicable to cases where the admission to the programme is less than 10.

Mini-project work – Extensive Survey Project: Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications.

Based on the ability/abilities of the student/s and recommendations of the mentor Mini- project can be assigned to a group having not more than 10 students.

CIE procedure for Mini-project – Extensive Survey Project:

The CIE marks shall be awarded by a committee consisting of the Head of the Department and two faculty members of the Department, one of them being the Guide. The CIE marks awarded for the Mini-project work shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

No SEE component for Mini-Project.

VII semester Class work and Research Internship /Industry Internship (21INT82)

Swapping Facility

Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate research internship/ industry internship after the VI semester**.**

(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the program.

Elucidation:

At the beginning of IV years of the program i.e., after VI semester, VII semester classwork and VIII semester Research Internship /Industrial Internship shall be permitted to be operated simultaneously by the University so that students have ample opportunity for an internship. In other words, a good percentage of the class shall attend VII semester classwork and a similar percentage of others shall attend to Research Internship or Industrial Internship.

Research/Industrial Internship shall be carried out at an Industry, NGO, MSME, Innovation center, Incubation center, Start-up, center of Excellence (CoE), Study Centre established in the parent institute and /or at reputed research organizations/institutes.

The mandatory Research internship /Industry internship is for 24 weeks. The internship shall be considered as a head of passing and shall be considered for the award of a degree. Those, who do not take up/complete the internship shall be declared to fail and shall have to complete it during the subsequent University examination after satisfying the internship requirements.

INT21INT82Research Internship/ Industry Internship/Rural Internship

Research internship:A research internship is intended to offer the flavor of current research going on in the research field. It helps students get familiarized with the field and imparts the skill required for carrying out research.

Industryinternship: Isan extended period of work experience undertaken by students to supplement their degree for professional development. It also helps them learn to overcome unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with contingencies helps students recognize, appreciate, and adapt to organizational realities by tempering their knowledge with practical constraints.

The faculty coordinator or mentor has to monitor the students' internship progress and interact with them to guide for the successful completion of the internship.

The students are permitted to carry out the internship anywhere in India or abroad. University shall not bear any expenses incurred in respect of internship.

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Swappable VII and VIII SEMESTER

VII SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	PCC 21CV71	Quantity Survey and Contract Management	TD: Civil Engg PSB: Civil Engg	2	2	0		3	50	50	100	3
2	PCC 21CV72	Construction Technology for Substructure and Super Structures	TD: Civil Engg PSB: Civil Engg	2	0	0		3	50	50	100	2
3	PEC 21CV73X	Professional elective Course-II	TD: Civil Engg PSB: Civil Engg	3	0	0		3	50	50	100	3
4	PEC 21CV74X	Professional elective Course-III	TD: Civil Engg PSB: Civil Engg	3	0	0		3	50	50	100	3
5	OEC 21CV75X	Open elective Course-II	Concerned Department	3	0	0		3	50	50	100	3
6	Project 21CVP76	Project work	TD: Civil Engg PSB: Civil Engg	Two contact hours /week for interaction between the faculty and students.				3	100	100	200	10
								Total	**350**	**350**	**700**	**24**

VIII SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	Seminar 21CV81		Technical Seminar	TD: Civil Engg PSB: Civil Engg	One contact hour /week for interaction between the faculty and students.				--	100	--	100	01
2	INT 21INT82		Research Internship/ Industry Internship	TD: Civil Engg PSB: Civil Engg	Two contact hours /week for interaction between the faculty and students.				03 (Batch wise)	100	100	200	15
3	NCMC	21NS83	National Service Scheme (NSS)	NSS	Completed during the intervening period of III semester toVIII semester.				--	50	50	100	0
		21PE83	Physical Education (PE) (Sports and Athletics)	PE									
		21YO83	Yoga	Yoga									
									Total	**250**	**150**	**400**	**16**

Professional Elective - II

21CV721	Advanced Design of RCC and Steel Structures	21CV724	Solid Waste Management
21CV722	Advanced Geotechnical Engineering	21CV725	Design of Hydraulic Structures
21CV723	Pavement Materials and Construction	21CV726	Repair, Retrofitting and Rehabilitation of Structures

Professional Elective - III

21CV731	Earthquake Engineering	21CV734	Air Pollution and Control
21CV732	Ground Improvement Techniques	21CV735	Open Channel Hydraulics
21CV733	Pavement Design	21CV736	Design of Masonry Structures

Open Electives - II offered by the Department to other Department students			
21CV741	Finite Element Method	21CV744	Intelligent Transportation Systems
21CV742	Numerical Methods and Applications		
21CV743	Environmental Protection and Management		

Note: PCC: Professional Core Course, **PEC:** Professional Elective Courses, **OEC**–Open Elective Course, **AEC** –Ability Enhancement Courses.
L –Lecture, T – Tutorial, P- Practical / Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Note: VII and VIII semesters of IV year of the programme

(1) Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate research internship/ industry internship after the VI semester**.**

(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the program.

PROJECT WORK (21XXP75): The objective of the Project work is

(i) To encourage independent learning and the innovative attitude of the students.
(ii) To develop interactive attitude, communication skills, organization, time management, and presentation skills.
(iii) To impart flexibility and adaptability.
(iv) To inspire team working.
(v) To expand intellectual capacity, credibility, judgment and intuition.
(vi) To adhere to punctuality, setting and meeting deadlines.
(vii) To install responsibilities to oneself and others.
(viii) To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

CIE procedure for Project Work:

(1) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work, shall be based on the evaluation of the project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(2) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable. The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE procedure for Project Work: SEE for project work will be conducted by the two examiners appointed by the University. The SEE marks awarded for the project work shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25.

TECHNICAL SEMINAR (21XXS81): The objective of the seminar is to inculcate self-learning, present the seminar topic confidently, enhance communication skill, involve in group discussion for the exchange of ideas. Each student, under the guidance of a Faculty, shall choose, preferably, a recent topic of his/her interest relevant to the program of Specialization.

(i) Carry out a literature survey, and systematically organize the content. **(ii)** Prepare the report with your own sentences, avoiding a cut and paste act. **(iii)**Type the matter to acquaint with the use of Micro-soft equation and drawing tools or any such facilities. **(iv)** Present the seminar topic orally and/or through PowerPoint slides. **(v)** Answer the queries and involve in debate/discussion. (**vi)** Submit a typed report with a list of references.

The participants shall take part in the discussion to foster a friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Evaluation Procedure:

The CIE marks for the seminar shall be awarded (based on the relevance of the topic, presentation skill, participation in the question and answer session, and quality of report) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three teachers from the department with the senior-most acting as the Chairman.

Marks distribution for CIE of the course:

Seminar Report:50 marks
Presentation skill:25 marks
Question and Answer: 25 marks. ■No SEE component for Technical Seminar

Non–credit mandatory courses (NCMC):

National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE, and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequently to earn the qualifying CIE marks subject to the maximum program period.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of a degree.

B. E. (Common to all branches)

Choice Based Credit System (CBCS) and Outcome-Based Education (OBE)

SEMESTER - III

TRANSFORM CALCULUS, FOURIER SERIES AND NUMERICAL TECHNIQUES			
Course Code	**21MAT 31**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course objectives: The goal of the course Transform Calculus, Fourier series and Numerical techniques 21MAT 31 is

- To have an insight into solving ordinary differential equations by using Laplace transform techniques
- Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis.
- To enable the students to study Fourier Transforms and concepts of infinite Fourier Sine and Cosine transforms and to learn the method of solving difference equations by the z-transform method.
- To develop proficiency in solving ordinary and partial differential equations arising in engineering applications, using numerical methods

Teaching-Learning Process (General Instructions):

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied mathematical skills.
2. State the need for Mathematics with Engineering Studies and Provide real-life examples.
3. Support and guide the students for self–study.
4. You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students' progress.
5. Encourage the students for group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lecture activity).
   - As additional examples (post-lecture activity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution for some exercises (post-lecture activity).

Module-1: Laplace Transform

Definition and Laplace transforms of elementary functions (statements only). Problems on Laplace's Transform of $e^{at}f(t)$, $t^n f(t)$, $\frac{f(t)}{t}$. Laplace transforms of Periodic functions (statement only) and unit-step function – problems.

Inverse Laplace transforms definition and problems, Convolution theorem to find the inverse Laplace transforms (without Proof) problems. Laplace transforms of derivatives, solution of differential equations. **(8 Hours)**

Self-study: Solution of simultaneous first-order differential equations. **(RBT Levels: L1, L2 and L3)**	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation
Module-2: Fourier Series	
Introduction to infinite series, convergence and divergence. Periodic functions, Dirichlet's condition. Fourier series of periodic functions with period 2π and arbitrary period. Half range Fourier series. Practical harmonic analysis. **(8 Hours)** **Self-study:** Convergence of series by D'Alembert's Ratio test and, Cauchy's root test. **(RBT Levels: L1, L2 and L3)**	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation
Module-3: Infinite Fourier Transforms and Z-Transforms	
Infinite Fourier transforms definition, Fourier sine and cosine transforms. Inverse Fourier transforms, Inverse Fourier cosine and sine transforms. Problems. Difference equations, z-transform-definition, Standard z-transforms, Damping and shifting rules, Problems. Inverse z-transform and applications to solve difference equations. **(8 Hours)** **Self Study**: Initial value and final value theorems, problems. **(RBT Levels: L1, L2 and L3)**	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation
Module-4: Numerical Solution of Partial Differential Equations	
Classifications of second-order partial differential equations, finite difference approximations to derivatives, Solution of Laplace's equation using standard five-point formula. Solution of heat equation by Schmidt explicit formula and Crank- Nicholson method, Solution of the Wave equation. Problems. **(8 Hours)** **Self Study**: Solution of Poisson equations using standard five-point formula. **(RBT Levels: L1, L2 and L3)**	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation
Module-5: Numerical Solution of Second-Order ODEs and Calculus of Variations	
Second-order differential equations - Runge-Kutta method and Milne's predictor and corrector method. (No derivations of formulae). Calculus of Variations: Functionals, Euler's equation, Problems on extremals of functional. Geodesics on a plane, Variational problems. **(8 Hours)** **Self Study:** Hanging chain problem **(RBT Levels: L1, L2 and L3)**	
Course outcomes: After successfully completing the course, the students will be able : ➢ To solve ordinary differential equations using Laplace transform. ➢ Demonstrate the Fourier series to study the behaviour of periodic functions and their applications in system communications, digital signal processing and field theory. ➢ To use Fourier transforms to analyze problems involving continuous-time signals and to apply Z-Transform techniques to solve difference equations ➢ To solve mathematical models represented by initial or boundary value problems involving partial differential equations ➢ Determine the extremals of functionals using calculus of variations and solve problems arising in dynamics of rigid bodies and vibrational analysis.	

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

First test at the end of 5th week of the semester

Second test at the end of the 10th week of the semester

Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

First assignment at the end of 4th week of the semester

Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

The question paper will have ten questions. Each question is set for 20 marks. Marks scored shall be proportionally reduced to 50 marks

There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books:

1. **B. S. Grewal**: "Higher Engineering Mathematics", Khanna publishers, 44th Ed.2018
2. **E. Kreyszig**: "Advanced Engineering Mathematics", John Wiley & Sons, 10th Ed. (Reprint), 2016.

Reference Books

1. **V. Ramana:** "Higher Engineering Mathematics" McGraw-Hill Education, 11th Ed.
2. **Srimanta Pal & Subodh C. Bhunia:** "Engineering Mathematics" Oxford University Press, 3rd Reprint, 2016.
3. **N.P Bali and Manish Goyal**: "A textbook of Engineering Mathematics" Laxmi Publications, Latest edition.
4. **C. Ray Wylie, Louis C. Barrett:** "Advanced Engineering Mathematics" McGraw – Hill Book Co.Newyork, Latest ed.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** "Engineering Mathematic for Semester I and II", Mc-Graw Hill Education(India) Pvt. Ltd 2015.
6. **H.K.Dass and Er. Rajnish Verma:** "Higher Engineering Mathematics" S.Chand Publication (2014).
7. **James Stewart: "**Calculus" Cengage publications, 7th edition, 4th Reprint 2019.

Web links and Video Lectures (e-Resources):
• http://.ac.in/courses.php?disciplineID=111 • http://www.class-central.com/subject/math(MOOCs) • http://academicearth.org/ • http://www.bookstreet.in. • VTU e-Shikshana Program • VTU EDUSAT Program
Activity-Based Learning (Suggested Activities in Class)/ Practical Based learning • Quizzes • Assignments • Seminars

III Semester

Geodetic Engineering			
Course Code	**21CV32**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:2:0	SEE Marks	50
Total Hours of Pedagogy	50	Total Marks	100
Credits	4	Exam Hours	03

Course objectives:

- Provide basic knowledge about principles of surveying for location, design and construction of engineering projects
- Develop skills for using surveying instruments including, levelling instruments, plane tables, theodolite, compass
- Make students to familiar with cooperative efforts required in acquiring surveying data and applying fundamental concepts to eliminate errors and set out the works
- Provide information about new technologies that are used to abstracting the information of earth surface

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. The survey of India topomap has to be shared with students and few exercise must be given
2. The satellite imagery has to be procured and shared with students
3. The manual for conducting field survey has to be provided
4. The online courses available should be shared with students
5. YouTube videos
6. Power point presentations

Module-1

Introduction to Surveying: Importance of surveying in Civil Engineering, Concepts of plane and geodetic surveying Principles of surveying –Plans and maps – Surveying equipment's, Meridians, Bearings, Dip, Declination, Local attraction, Calculation of bearings and included angles. Compass surveying and Plane Table Surveying

Compass surveying: Prismatic and surveyor's compasses, temporary adjustments.

Plane Table Surveying: plane table and accessories, advantages and disadvantages of plane table survey, method of plotting - radiation, intersection, traversing, resection, two point and three point method

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-2

Levelling – Principles and basic definitions – Types of Levels – Types of adjustments and objectives – Types of levelling – Simple, Differential, Fly, Reciprocal, Profile, Cross sectioning – Booking of levels – Rise & fall and H. I methods (Numerical)

Areas and volumes: Measurement of area – by dividing the area into geometrical figures, area from offsets, mid ordinate rule, trapezoidal and Simpsons one third rule, area from co-ordinates, introduction to planimeter, digital planimeter. Measurement of volumes-trapezoidal and prismoidal formula.

Teaching-Learning	Chalk and talk, PowerPoint Presentation, YouTube videos

Process	

Module-3

Theodolite Surveying: Theodolite and types, fundamental axes and parts of theodolite, temporary adjustments of transit theodolite, Horizontal and Vertical angle measurements by repetition and reiteration Trigonometric levelling: Single and Double plane for finding elevation of objects Computation of distances and elevations using Tacheometric method.

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-4

Curve Surveying: Curves – Necessity – Types, Simple curves, Elements , Designation of curves, Setting out simple curves by linear methods (numerical problems on offsets from long chord & chord produced method), Setting out curves by Rankine's deflection angle method (numerical problems). Compound curves, Elements, Design of compound curves, Setting out of compound curves (numerical problems). Reverse curve between two parallel straights (numerical problems on Equal radius and unequal radius). Transition curves Characteristics, numerical problems on Length of Transition curve, Vertical curves –Types – (theory).

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-5

Photogrammetry and aerial survey: Introduction, definitions, basics principles, methods, importance of scale, height, applications.

Remote sensing: Introduction, Principle of Remote sensing, EMR, types, resolutions, types of satellites, type of sensors, LIDAR, visual and digital image processing and its applications. **Global Positioning System:** Definition, Principles of GPS and applications. Geographical Information System: Introduction and principle of Geographical Information System, components of GIS, applications

Advanced instrumentation in surveying: classification, measuring principles, Electronic theodolite, EDM, Total Station, Drones

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

LABORATORY EXPERIMENTS

1.	Study of various instruments used for surveying, namely chain, tape, Compass,
2.	Dumpy level, Auto-level, Theodolite, Tacheometer, Total station and GPS. To find the distance between two points shown in the field using method of pacing, chaining and taping.
3.	To set regular geometric figures (Hexagon and Pentagon) using chain tape and accessories.
4.	To set regular geometric figures (Hexagon and Pentagon) using prismatic compass, given the bearing of one line.
5.	Study of use of Dumpy level and to determine the different in elevation between two points by differential levelling using Dumpy level
6.	To find the true difference in elevation between two points situated far apart by using Reciprocal levelling.

7.	Trigonometrical levelling: Single plane method and Double plane method
8.	Measurement of horizontal angle using theodolite by: i) Method of Repetition and ii) Reiteration method.
9.	Setting simple circular curve-Instrumental method,
10.	Setting compound curve using theodolite
11.	Plane table : Setting, orientation, radiation, intersection
12.	Demo: Total station, GPS

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

1. Execute survey using compass and plane table
2. Find the level of ground surface and Calculation of area and volumes
3. Operate theodolite for field execution
4. Estimate the capacity of reservoir
5. Interpret satellite imageries

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 02/03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will have ten questions. Each question is set for 20 marks. Marks scored shall be proportionally scaled down to 50 Marks
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Books

1. Surveying & levelling Vol. I ,II & III, B. C. Punmia, Laxmi Publications; seventeenth edition (2016)
2. Advanced Surveying: Total Station, GPS, GIS & Remote Sensing by Pearson 2017 by GopiSatheesh, R.Sathikumar, N. Madhu
3. Surveying Vol.I& II, S. K. Duggal, McGraw Hill Education; Fourth edition (2017)

4. Surveying and Levelling, R. Subramanian , second edition, 2012, Oxford University Press; 5. Engineering Surveying, Schofield and Breach, 6th edition, Butterworth-Heinemann (Elsevier publication, 2007) 6. Surveying , A Banister, S Raymond, R Baker, 7th edition, Pearson , New Delhi	
Web links and Video Lectures (e-Resources):	
• NPTEL courses	
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning	

III Semester

STRENGTH OF MATERIALS			
Course Code	**21CV33**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2+2+2+0	SEE Marks	50
Total Hours of Pedagogy	50	Total Marks	100
Credits	4	Exam Hours	03 hrs

Course objectives: This course will enable students

1. To understand the basic concepts of the stresses and strains for different materials and strength of structural elements.
2. To know the development of internal forces and resistance mechanism for one dimensional and two-dimensional structural elements.
3. To analyse and understand different internal forces and stresses induced due to representative loads on structural elements.
4. To determine slope and deflections of beams.
5. To evaluate the behaviour of torsion members, columns and struts.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Blackboard teaching/PowerPoint presentations (if needed)
2. Regular review of students by asking questions based on topics covered in the class.

Module-1

Simple Stresses and Strains: Introduction, Properties of Materials, Stress, Strain, Hook's law, Poisson's Ratio, Stress – Strain Diagram for structural steel, Principles of superposition, Total elongation of tapering bars of circular and rectangular cross sections. Composite section, Volumetric strain, expression for volumetric strain, Elastic constants, relationship among elastic constants (No Numerical), Thermal stress and strains

Compound stresses: Introduction, Stress components on inclined planes, General two-dimensional stress system, Principal planes and stresses, maximum shear stresses and their planes (shear planes). Compound stress using Mohr's circle method.

Teaching-Learning Process	1.Blackboard teaching/PowerPoint presentations (if needed) 2.Regular review of students by asking questions based on topics covered in the class.

Module-2

Bending moment and shear force diagrams in beams: Definition of shear force and bending moment, Sign convention, Relationship between loading, shear force and bending moment, Shear force and bending moment equations, development of Shear Force Diagram(SFD) and Bending Moment Diagram (BMD) with salient values for cantilever, simply supported and overhanging beams for point loads, UDL(Uniformly Distributed Load), UVL(Uniformly Varying Load) and Couple.

Teaching-Learning Process	1.Blackboard teaching/PowerPoint presentations (if needed) 2.Regular review of students by asking questions based on topics covered in the class.

Module-3

	Bending stress in beams: Introduction – Bending stress in beam, Pure bending, Assumptions in simple bending theory, derivation of Simple bending equation (Bernoulli's equation), modulus of rupture, section modulus, Flexural rigidity, Problems **Shear stress in beams:** Derivation of Shear stress intensity equations, Derivation of Expressions of the shear stress intensity for rectangular, triangular and circular cross sections of the beams. Problems on calculation of the shear stress intensities at various critical levels of T, I and Hollow rectangular cross sections of the beam.	
	Teaching-Learning Process	1.Blackboard teaching/PowerPoint presentations (if needed) 2.Regular review of students by asking questions based on topics covered in the class.
	Module-4	
	Torsion: Twisting moment in shafts, simple torque theory, derivation of torsion equation, tensional rigidity, polar modulus, shear stress variation across solid circular and hollow circular sections, Problems **Thin cylinders:** Introduction: Longitudinal, circumferential (hoop) stress in thin cylinders. Expressions for longitudinal and circumferential stresses. Efficiency of longitudinal and circumferential joints. Problems on estimation of change in length, diameter and volume when the thin cylinder subjected to internal fluid pressure. **Thick cylinders:** Concept of Thick cylinders Lame's equationsapplicable to thick cylinders with usual notations, calculation of longitudinal, circumferential and radial stresses – simple numerical examples. Sketching the variation of radial stress (pressure) and circumferential stress across the wall of thick cylinder. U	
	Teaching-Learning Process	1.Blackboard teaching/PowerPoint presentations (if needed) 2.Regular review of students by asking questions based on topics covered in the class.
	Module-5	
	Elastic stability of columns: Introduction – Short and long columns, Euler's theory on columns, Effective length, slenderness ratio, radii of gyration, buckling load, Assumptions, derivations of Euler's Buckling load for different boundary conditions, Limitations of Euler's theory, Rankine's formula and related problems. **Deflection of determinate Beams:** Introduction, Elastic curve –Derivation of differential equation of flexure, Sign convention, Slope and deflection using Macaulay's method for statically determinate beams subjected to various vertical loads, moment, couple and their combinations. Numerical problems.	
	Teaching-Learning Process	1.Blackboard teaching/PowerPoint presentations (if needed) 2.Regular review of students by asking questions based on topics covered in the class.

LABORATORY

1. Dimensionality of bricks, Water absorption, Initial rate of absorption
2. Specific gravity of coarse and fine aggregate
3. Fineness modulus of Fine and Coarse aggregate
4. Compressive strength tests on building blocks (brick, solid blocks and hollow blocks)
5. Tension test on Mild steel and HYSD bars
6. Compression test on HYSD, Cast iron
7. Bending Test on Wood under two-point loading.

8. Shear Test on Mild steel – single and double shear
9. Impact test on Mild Steel (Charpy& Izod)

Course outcome (Course Skill Set)

After completion of the course, students will be able to

1. Evaluate the behaviour when a solid material is subjected to various types of forces (namely Compressive, Tensile, Thermal, Shear, flexure, Torque, internal fluid pressure) and estimate stresses and corresponding strain developed. (L3)
2. Estimate the forces developed and draw schematic diagram for stresses, forces, moments for simple beams with different types of support and are subjected to various types of loads (L3).
3. Evaluate the behaviour when a solid material is subjected to Torque and internal fluid pressure and estimate stresses and corresponding strain developed. (L3)
4. Distinguish the behaviour of short and long column and calculate load at failure & explain the behaviour of spring to estimate deflection and stiffness (L3)
5. Examine and Evaluate the mechanical properties of various materials under different loading conditions

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 02/03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory

component of IPCC for **20 marks**.

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SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will have ten questions. Each question is set for 20 marks. Marks scorded shall be proportionally scaled down to 50 Marks
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

Suggested Learning Resources:

Books

1.Timoshenko and Young, “Elements of Strength of Materials” ,EastWest Press, 5t edition 2003

2.R. Subramanyam, “Strength of Materials”, Oxford University Press, 3rd Edition -2016

3.B.C Punmia Ashok Jain, Arun Jain, “Strength of Materials”, Laxmi - 2018-22 Publications, 10th Edition-2018

Web links and Video Lectures (e-Resources):

1.Strength of Materials web course by IIT Roorkee https://nptel.ac.in/courses/112107146/

2.Strength of Materials video course by IIT Kharagpur https://nptel.ac.in/courses/105105108/

3.Strength of Materials video course by IIT Roorkee https://nptel.ac.in/courses/112107147/18

4.All contents organized http://www.nptelvideos.in/2012/11/strengthof-materials-prof.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Seminars/Quizz(To assist in GATE Preparations
- Demonstrations in Lab
- Self Study on simple topics
- Simple problems solving using Excel
- Virtual Lab Experiments

22.09.2022 updated

Semester III

: **Earth Resources and Engineering**			
Course Code	21CV34	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- This course will enable students;

  1. To understand the importance of earth's dynamic interior in civil engineering and Geo Hazard mitigation and management
  2. To analyse the physical characteristics of the rocks and Minerals for its suitable application in Engineering
  3. To evaluate earth Process for providing sustainable management and Development through Geoengineering.
  4. Subsurface Exploration for providing safe and suitable site condition and Earth Resources for Reengineering activities
  5. To application of modern tools and techniques in Earth Resources Management and.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

- Chalk and Talk method.
- Show Video/animation films to explain earth dyanamics and influence of geology in prime civil constructions
- Encourage collaborative (Group Learning) Learning in the class
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking process such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Module /unit – 01 – Introduction, scope of earth science in Engineering, 8 hrs
Geohazards and disasters, Mitigation and management

Earths internal dynamics ,Plate tectonics, Earth quakes types, causes iso-seismal line, seismic zonation map, seismic proof structures, Numerical problems on location of epicenter; volcanic eruption, types, causes, ; landslides, causes types, preventive measures; tsunamis causes consequences, mitigation;cyclones, causes management

Teaching-Learning Process	• chalk and talk method, • power point presentation. • Case studies • Field visits

Module-2	
Earth Resources **8hrs** Minerals -Industrial, rock forming and ore minerals. Physical properties, composition and uses Rocks as a construction materials- physical properties, texture, composition, applications for aggregate, decorative (facing/polishing), railway ballast, rocks for masonry work, monumental/architecture, rocks as aquifers, water bearing properties igneous, sedimentary	
Teaching-Learning Process	• Chalk and talk method, • Power point presentation and Animated vedeos • Case studies • Field visits experience the real world examples
Module-3	
Surface investigation for Civil Engineering projects **8hrs** Weathering, type, causes, soil insitu, drifted soil, soil profile, soil mineralogy , structure, types of soil, Black cotton soil v/s Lateritic soil; effects of weathering on monumental rocks, River morphology and basin investigation for engineering Projects like earthen dam, gravity dam, arch dam, features of river erosion, deposition and their influences on river valley projects, morphometric analysis of river basin, selection of site for artificial recharge,, interlinking of river basins, coastal process and landforms, sedimentation /siltation, erosion	
Teaching-Learning Process	• Chalk and talk method, • Power point presentation and Animated vedeos • Case studies • Field visits experience the real world examples
Module-4	
Subsurface investigation for deep foundation **8hrs** Borehole data(and problems), Dip and strike, and outcrop problems(numerical problem geometrical/ simple trigonometry based), Electrical Resistivity meter, depth of water table, (numerical problems) seismic studies, faults, folds, unconformity, joints types, recognitionand their significance in Civil engineering projects like tunnel project, dam project, , Ground improvements like rock bolting, rock jointing, grouting	
Teaching-Learning Process	• Chalk and talk method, • Power point presentation and Animated vedeos • Case studies • Field visits experience the real world examples
Module-5	
Geo-tools and techniques for civil Engineering Applications **7hrs** Toposheets , Remote sensing and GIS. Photogrammetry (scale, flight planning, overlap, elevation effects, interpretation keys, numericals on flight, planning scale , elevation, flyimg height, ….), GPS,, Ground Penetrating Radas (GPR), Drone, and their applications	
Teaching-Learning Process	• Chalk and talk method, • Power point presentation and Animated videos • Case studies • Field visits and research institutes experience the real world examples

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Apply geological knowledge in different civil engineering practice.
2. Students will acquire knowledge on durability and competence of foundation rocks, and confidence enough to use the best building materials.
3. competent enough to provide services for the safety, stability, economy and life of the structures that they construct
4. Able to solve various issues related to ground water exploration, build up dams, bridges, tunnels which are often confronted with ground water problems
5. Intelligent enough to apply GIS, GPS and remote sensing as a latest tool in different civil engineering for safe and solid construction.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks. Marks scored out of 100, shall be proportionally reduced to 50 marks
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=aTVDiRtRook&list=PLDF5162B475DD915F
- https://www.youtube.com/watch?v=EBiLLJAxBuU&index=2&list=PLDF5162B475DD915F
- https://www.youtube.com/watch?v=sTY-ao4RZck&list=PLDF5162B475DD915F&index=3
- https://nptel.ac.in/courses
- https://youtu.be/fvoYHzAhvVM
- https://youtu.be/aTVDiRtRook

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- https://www.earthsciweek.org/classroom-activities
- Field Visits
- https://serc.carleton.edu/NAGTWorkshops/hazards/events/12262004.html?serc_source=recommendation
- https://serc.carleton.edu/NAGTWorkshops/visualization/examples/CBezanson.html?serc_source=recommendation
- https://serc.carleton.edu/NAGTWorkshops/coursedesign/goalsdb/14712.html

Textbooks -

1. Engineering Geology, by Parthasarathy et al, Wiley publications
2. A textbook of Engineering Geology by Chenna Kesavulu, Mac Millan India Ltd
3. Principle of Engineering Geology, by K.M. Bangar, Standard publishers
4. Physical and Engineering Geology, by S.K. Garg, Khanna publishers
5. Principles of Engineering Geology, by KVGK Gokhale, BS Publications

Reference books –

1. Introduction to Environmental Geology by Edward A Keller, Pearson publications.
2. Engineering Geology and Rock Mechanics B. P. Verma, Khanna publishers
3. Principles of Engineering Geology and Geotechnics, Krynine and Judd, CBS Publications

COMPUTER AIDED BUILDING PLANNING AND DRAWING			
Course Code	**21CVL35**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0+0+2+0	SEE Marks	50
Credits	01	Exam Hours	03 hrs

Course objectives:

Provide students with understanding

1. Gain skill set to prepare Computer Aided Engineering Drawings
2. Understanding the details of construction of different building elements
3. Visualize the completed form of the building and the intricacies of construction based on the engineering drawings
4. Get familiarization of practices used in Industry

Sl.NO	Experiments
	Module 1
1	**Drawing Basics:** Selection of scales for various drawings, thickness of lines, dimensioning, abbreviations and conventional representations as per IS:962.
2	**Simple Engineering Drawings with CAD** Drawing Tools**:** Lines Circle, Arc, Poly line, Multiline, Polygon, Rectangle, Spline, Ellipse, Modify tools: Erase, Copy, Mirror, Offset, Array, Move, Rotate, Scale, Stretch, Lengthen, Trim, Extend, Break, Chamfer and Fillet, Using Text: Single line text, Multiline text, Spelling, Edit text, Special Features: View tools, Layers concept, Dimension tools, Hatching, Customizing Toolbars, Working with multiple drawings.
	Module 2
3	**Drawings of Different Building Elements:** Following drawings are to be prepared for the data given using CAD Software a) Cross section of Foundation, masonry wall, RCC columns with isolated & combined footings. b) Different types of bonds in brick masonry. c) Different types of staircases – Dog legged, Open well, d) Lintel and chajja. e) RCC Slabs and beams. f) Cross section of a pavement. g) Septic Tank and sedimentation Tank. h) Layout plan of Rainwater recharging and harvesting system. i) Cross sectional details of a road for a Residential area with provision for all services. j) Steel truss (connections Bolted). **Note:**Students should sketch to dimension the above in a sketch book before doing the computer drawing.

Module 3	
4	**Building Drawings :** Principles of planning, Planning regulations and building bye-laws, factors affecting site selection, Functional planning of residential and public buildings, design aspects for different public buildings. Recommendations of NBC. Drawing of plan, elevation and sectional elevation including electrical, plumbing and sanitary services using CAD software for 1. Single and double story residential building. 2. Hostel building. 3. Hospital building. 4. School building. Submission drawing (sanction drawing)of two storied residential building with access to terrace including all details and statements as per the local bye-laws Industry Applications : 3D Modelling and Rendering, 2D Animation, Construction site Simulation **Note:** . Students should sketch to dimension the above in a sketch book before doing the computer drawing . One compulsory field visit/exercise to be carried out. . Single line diagrams to be given in the examination.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Prepare, read and interpret the drawings in a professional set up.
2. Know the procedures of submission of drawings and Develop working and submission drawings for building.
3. Plan and design of residential or public building as per the given requirements.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination(SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly

by examiners.
General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Question paper pattern:

- There will be four full questions with sub divisions if necessary from Module2 with each full question carrying twenty five marks. Students have to answer any two questions.
- There will be two full questions from Modulus 3 with each full question carrying fifty marks. Students have to answer any one question. The conduction of examination and question paper format of should be in line of 1st year CAED drawing. It's drawing paper but the exam will be conducted by batches in the computer labs. Question paper should be given in batches.

Suggested Learning Resources:

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Textbook:

1. MG Shah, CM Kale, SY Patki, "Building drawing with an integrated approach to Built Environment Drawing", Tata McGraw Hill Publishing co. Ltd, New Delhi.
2. Gurucharan Singh, "Building Construction", Standard Publishers, & distributors, New Delhi.
3. Malik RS and a Meo GS, "Civil Engineering Drawing", Asian Publishers/Computech Publication Pvt Ltd

Reference Books:

1. Time Saver Standard by Dodge F.W, F.W Dodge Corp.
2. IS: 962-1989 (Code of practice for architectural and building drawing).
3. National Building Code, BIS, New Delhi.

SAMPLE TEMPLATE

III/IV Semester

Constitution of India and Professional Ethics (CIP)

Course Code	**21CIP37/47**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:2:0:0	SEE Marks	50
Total Hours of Pedagogy	15 Hours	Total Marks	100
Credits	01	Exam Hours	01 Hour

Course objectives: This course will enable the students

- To know the fundamental political structure & codes, procedures, powers, and duties of Indian government institutions, fundamental rights, directive principles, and the duties of citizens.
- To understand engineering ethics and their responsibilities, identify their individual roles and ethical responsibilities towards society.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- ✓ Teachers shall adopt suitable pedagogy for effective teaching - learning process. The pedagogy shall involve the combination of different methodologies which suit modern technological tools and software's to meet the present requirements of the Global employment market.
  - (i) Direct instructional method (Low /Old Technology),
  - (ii) Flipped classrooms (High/advanced Technological tools),
  - (iii) Blended learning (combination of both),
  - (iv) Enquiry and evaluation based learning,
  - (v) Personalized learning,
  - (vi) Problems based learning through discussion,
  - (vii) Following the method of expeditionary learning Tools and techniques,
- **1.** Apart from conventional lecture methods, various types of innovative teaching techniques through videos, animation films may be adapted so that the delivered lesson can enhance the students in theoretical applied and practical skills in teaching of 21CIP39/49 in general.

Module - 1

Introduction to Indian Constitution: Definition of Constitution, Necessity of the Constitution, Societies before and after the Constitution adoption. Introduction to the Indian constitution, Making of the Constitution, Role of the Constituent Assembly. Preamble of Indian Constitution & Key concepts of the Preamble. Salient features of India Constitution.

Teaching-Learning Process	Chalk and talk method, Videos, Power Point presentation to teach. Creating real time stations in classroom discussions, Giving activities and assignments (Connecting Campus & community with administration real time situations).

Module - 2

Fundamental Rights (FR's), Directive Principles of State Policy (DPSP's) and Fundamental Duties (FD's) : Fundamental Rights and its Restriction and limitations in different Complex Situations. DPSP's and its present relevance in Indian society. Fundamental Duties and its Scope and significance in Nation building.

Teaching-Learning Process	Chalk and talk method, Videos, Power Point presentation to teach. Creating real time stations in classroom discussions, Giving activities and assignments (Connecting Campus & community with administration real time situations).

Module - 3

Union Executive : Parliamentary System, Union Executive – President, Prime Minister, Union Cabinet, Parliament - LS and RS, Parliamentary Committees, Important Parliamentary Terminologies. Supreme Court of India, Judicial Reviews and Judicial Activism.

Teaching-Learning Process	Chalk and talk method, Videos, Power Point presentation to teach. Creating real time stations in classroom discussions, Giving activities and assignments (Connecting Campus & community with administration real time situations).

Module - 4	
State Executive & Elections, Amendments and Emergency Provisions: State Executive, Election Commission, Elections & Electoral Process. Amendment to Constitution (Why and How) and Important Constitutional Amendments till today. Emergency Provisions.	
Teaching-Learning Process	Chalk and talk method, Videos, Power Point presentation to teach. Creating real time stations in classroom discussions, Giving activities and assignments (Connecting Campus & community with administration real time situations).
Module-5	
Professional Ethics: Definition of Ethics & Values. Professional & Engineering Ethics. Positive and Negative aspects of Engineering Ethics. Clash of Ethics, Conflicts of Interest. The impediments to Responsibility. Professional Risks, Professional Safety and liability in Engineering. Trust & Reliability in Engineering, Intellectual Property Rights (IPR's).	
Teaching-Learning Process	Chalk and talk method, Videos, Power Point presentation to teach. Creating real time stations in classroom discussions, Giving activities and assignments (Connecting Campus & community with administration real time situations).

Course outcome (Course Skill Set)

At the end of the course the student should :

CO 1: Have constitutional knowledge and legal literacy.

CO 2: Understand Engineering and Professional ethics and responsibilities of Engineers.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks that is 20 marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE and SEE taken together

Continuous Internal Evaluation:

Three Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject.

- The question paper will have 50 questions. Each question is set for 01 mark.
- SEE Pattern will be in MCQ Model (Multiple Choice Questions) for 50 marks. Duration of the examination is 01 Hour.

Textbook:

1. **"Constitution of India & Professional Ethics"** Published by Prasaranga or published on VTU website with the consent of the university authorities VTU Belagavi.

SAMPLE TEMPLATE

BE - **III/IV Semester – Common to all**

[illegible]			
[illegible] (Course Code)	21KSK39/49	[illegible]ದ [illegible]	50
[illegible] (Teaching Hours / Week (L:T:P: S)	0:2:0:1	[illegible]	50
[illegible] Total Hours of Pedagogy	25 [illegible]	[illegible]	100
[illegible] (Credits)	01	[illegible]	01 [illegible]

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[illegible] **(Teaching-Learning Process - General Instructions) :**

These are sample Strategies, which teacher can use to accelerate the attainment of the course outcomes.

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SAMPLE TEMPLATE

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(methods of CIE - MCQ, Quizzes, Open book test, Seminar or micro project)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The student has to obtain a minimum of 40% marks individually both in CIE and 35% marks in SEE to pass. Theory Semester End Exam (SEE) is conducted for 50 marks (01 hour duration). Based on this grading will be awarded.

Continuous Internal Evaluation:

Three Tests each of **20 Marks (duration 01 hour**)

a. First test at the end of 5th week of the semester
b. Second test at the end of the 10th week of the semester
c. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks : 1.** First assignment at the end of 4th week of the semester

2. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

3. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

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SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject.

1. The question paper will have 50 questions. Each question is set for 01 mark.

SEE Pattern will be in MCQ Model for 50 marks. Duration of the exam is 01 Hour.

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SAMPLE TEMPLATE

BE - III / IV Semester – Common to All

[illegible] – baLake Kannada (Kannada for Usage)

[illegible] – (Prescribed Textbook to Learn Kannada)

[illegible] (Course Code)	21KBK39/49	[illegible] (Continuous Internal Evaluation Marks)	50
[illegible] (Teaching Hours / Week (L:T:P: S)	0:2:0:1	[illegible] (Semester End Examination Marks)	50
[illegible] Total Hours of Pedagogy	25 [illegible]	[illegible] (Total Marks)	100
[illegible] (Credits)	01	[illegible] (Exam Hours)	01 [illegible]

[illegible] **(Course Learning Objectives):**

- To Create the awareness regarding the necessity of learning local language for comfortable and healthy life.
- To enable learners to Listen and understand the Kannada language properly.
- To speak, read and write Kannada language as per requirement.
- To train the learners for correct and polite conservation.

[illegible] **(Teaching-Learning Process - General Instructions) :**

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. [illegible].
2. [illegible].
3. [illegible].
1. [illegible].
2. [illegible].

Module-1

1. Introduction, Necessity of learning a local language. Methods to learn the Kannada language.
2. Easy learning of a Kannada Language: A few tips. Hints for correct and polite conservation, Listening and Speaking Activities
3. Key to Transcription.
4. [illegible], [illegible]/[illegible] – **Personal Pronouns, Possessive Forms, Interrogative words**

[illegible]	[illegible], [illegible], [illegible].

Module-2

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2. □□□□, □□□□□□□ □□□□□□ □□□□□□□□□ □□□□□□□□□□, □□□□□□□□□□□□□□□ **Qualitative, Quantitative and Colour Adjectives, Numerals**
3. **PÁgÀPÀ gÀÆ¥ÀUÀ¼ÀÄ ªÀÄvÀÄÛ «¨sÀQÛ ¥ÀævÀåAiÀÄUÀ¼ÀÄ – ¸À¥ÀÛ«Ä «¨sÀQÛ ¥ÀævÀåAiÀÄ – (D, CzÀÄ, CªÀÅ, C°è) Predictive Forms, Locative Case**

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Module-3

1. **ZÀvÀÄyð «¨sÀQÛ ¥ÀævÀåAiÀÄzÀ §¼ÀPÉ ªÀÄvÀÄÛ ¸ÀASÁåªÁZÀPÀUÀ¼ÀÄ - Dative Cases, and Numerals**
4. **¸ÀASÁåUÀÄtªÁZÀPÀUÀ¼ÀÄ ªÀÄvÀÄÛ §ºÀÄªÀZÀ£À £ÁªÀÄgÀÆ¥ÀUÀ¼ÀÄ - Ordinal numerals and Plural markers**
5. **£ÀÆå£À /¤µÉÃzsÁxÀðPÀ QæAiÀiÁ¥ÀzÀUÀ¼ÀÄ ªÀÄvÀÄÛ ªÀtð UÀÄtªÁZÀPÀUÀ¼ÀÄ**
   Defective / Negative Verbs and Colour Adjectives

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Module-4

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Permission, Commands, encouraging and Urging words (Imperative words and sentences)

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Accusative Cases and Potential Forms used in General Communication

3. "□□□□ □□□□□□ □□□□□□" □□□□□□ □□□□□□□□□□□□□□, □□□□□□□□□□□□□ □□□□□□ □□□□□□□□□□□□ □□□□□□□ □□□□□□ - Helping Verbs
   "iru and iralla", Corresponding Future and Negation Verbs
6. □□□□□□□ (ತರತಮ, □□□□□□ □□□□□ □□□□□□ □□□□□□ □□□□□ □□□□□□□□□□□ □□□□□□ □□□□□□□□□□□ ಪದಗಳ□□□□- Comparitive, Relationship, Identification and Negation Words

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Module-5

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2. □□, -□□,- □□,- □□□,- □□□□,- □□□□□,- □□,-□□, □□□□, □□□□□□□ □□□□□□□□□□□□□□□□□□ □□□□, □□□□□□□□□ □□□□□□ □□□□□□□□ □□□□ □□□□□□ □□□□□ - Formation of Past, Future and Present Tense Sentences with Verb Forms
3. **Kannada Vocabulary List :** □□□□□□□□□□□□□□ □□□□□□□□□□ □□□□□□ □□□□□□ - **Kannada Words in Conversation**

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□□□□□ □□□□□□□□□□: **course Outcomes (Course Skill** Set): At the end of the Course, The Students will be able

1. To understand the necessity of learning of local language for comfortable life.
2. To Listen and understand the Kannada language properly.
3. To speak, read and write Kannada language as per requirement.
4. To communicate (converse) in Kannada language in their daily life with kannada speakers.
5. To speak in polite conservation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation:

Three Tests each of **20 Marks (duration 01 hour**)

a. First test at the end of 5th week of the semester
b. Second test at the end of the 10th week of the semester
c. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks : 1.** First assignment at the end of 4th week of the semester

7. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

8. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

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SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject.

2. The question paper will have 50 questions. Each question is set for 01 mark.
3. SEE Pattern will be in MCQ Model for 50 marks. Duration of the exam is 01 Hour.

Textbook :

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Semester III

Problem Solving with Python			
Course Code	21CV381	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:2:0:0	SEE Marks	50
Total Hours of Pedagogy	15	Total Marks	100
Credits	1	Exam Hours	1 hr

Course objectives:

- To understand why Python is a useful scripting language for developers.
- To read and write simple Python programs
- To learn how to identify Python object types.
- To learn how to write functions and pass arguments in Python.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Python: Installing Python and Python packages, Managing virtual environments with venv module

Introduction to NumPy arrays:Array creation, indexing, data types, broadcasting, copies and views, universal functions, I/O with NumPy

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-2

Introduction to NumPy and SciPy:NumPy subpackages– linalg, fft, random, polynomials, SciPy subpackages– linalg, fftpack, integrate, interpolate, optimize

Introduction to Matplotlib: Plotting 2D graphs with Matplotlib, annotations, legend, saving plots to file, bar and pie charts, line plots.

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-3

Linear algebra using NumPy and SciPy:Solving linear simultaneous equations using NumPy and SciPy using numpy.linalg and scipy.linalg – solve, inverse, determinant, least square solution,

Linear algebra using NumPy and SciPy (continued): Decomposition using lu and cholesky.

Solving eigenvalue problems using NumPy and SciPy:Using numpy.linalg and scipy.linalg – eig, eigvals.

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-4	
Solving initial value problems for ODE systems using scipy.integrate subpackage – solve_ivp, RK45, LSODA. Numerical integration of functions using SciPy:Using scipy.integratesubpackage– Definite integral using Gaussian quadrature – quad and quadrature Numerical integration of fixed samples using scipy.integratesubpackage– Trapezoidal rule trapezoid, Simpson's 1/3 rule using Simpson, Romberg integration romb.	
Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos
Module-5	
Determining roots of equations using SciPyusing scipy.optimizesubpackage– Bisection method bisect, Brent's method brentq, Newton-Raphson method newton. Symbolic computing using SymPy and solving civil engineering problems using SymPy: Introduction, defining symbols, derivatives, integrals, limits, expression evaluation, expression simplification, solving equations, solving differential equations.	
Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Understand Python syntax and semantics and be fluent in the use of Python flow control and functions.
2. Demonstrate proficiency in handling Strings and File Systems.
3. Represent compound data using Python lists, tuples, Strings, dictionaries.
4. Read and write data from/to files in Python Programs

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

Three Tests (preferably in MCQ pattern with 20 questions) each of 20 Marks (duration 01 hour)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of 10 Marks

1. First assignment at the end of 4th week of the semester
2. Second assignment at the end of 9th week of the semester

Quiz/Group discussion/Seminar, any two of three suitably planned to attain the COs and POs for 20 Marks (duration 01 hours)

The sum of total marks of three tests, two assignments, and quiz /seminar/ group discussion will be out of 100 marks and shall be scaled down to 50 marks

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of 01 mark. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is 01 hour. The student has to secure minimum of 35% of the maximum marks meant for SEE.

Suggested Learning Resources:

Books

1. R. Nageswara Rao, "Core Python Programming", dreamtech

2. Python Programming: A Modern Approach, Vamsi Kurama, Pearson
3. Python Programming , Reema theraja, OXFORD publication

Web links and Video Lectures (e-Resources):

1. NumPy documentation at https://numpy.org/doc/
2. SciPy documentation at https://docs.scipy.org/doc/scipy/
3. Matplotlib documentation at https://matplotlib.org/stable/users/index
4. SymPy documentation at https://docs.sympy.org/latest/index.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Real world problem solving: Demonstration of projects developed using python language

Semester III

Microsoft Excel and Visual Basic for Applications			
Course Code	21CV382	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:2:0:0	SEE Marks	50
Total Hours of Pedagogy	15	Total Marks	100
Credits	1	Exam Hours	01 hr

Course objectives:

- To learn basic operations using excel
- To solve problems using functions in excel
- To design structural elements using excel and VB as a tool

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. The online courses available should be shared with students
2. YouTube videos
3. Power point presentations
4. Assignments to solve all the problems using excel and VB.

Module-1

Introduction to Microsoft Excel, Workbooks, Worksheets, User Interface – navigating the interface, entering data, implicit data types, setting cell data types, Basic operations – copy/cut, paste, paste special, row and cell references, using cell names, Simple built-in formulae, Copying and pasting formulae

Built-in formulae – Trigonometric, Logarithmic, Exponential, Statistical, Matrix operations such as transpose, multiplication, inverse etc.

Plotting charts of different types, bar and pie charts, scatter plots, legend, Using Log and Semilog scales, Customizing chart axes, Using multiple axes, Preparing contour plots, Annotating charts.

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-2

Introduction to Visual Basic for Applications, User Interface – VBA Editor, VBA toolbar, Developing simple functions in VBA – area of a circle, minimum cover to reinforcement in a beam as per IS 456, Calling user defined functions, Organizing code into modules.

Debugging VBA code using built-in debugger – breakpoints, watch variables, trace lines of code with run to cursor, step into, step over and step out.

Developing subroutines, calling subroutines, Differences between functions and subroutines, Scope of subroutines – Public and Private, Calling a subroutine

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-3

VBA data types, Working with data types, Enforcing defining types with Option Explicit, Defining, initializing and using arrays within functions/subroutines.

Commenting code, Long statements spanning multiple lines, Program flow control – Branching and looping, using conditional statements, Calling Worksheet functions in VBA.

Develop functions for simple civil engineering applications – Stability of gravity dams, analysis of

rectangular footings subjected to axial compression and bending about both axes, etc.

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-4

Table lookup – Lookup, Vlookup, Hlookup, Match, Index, VBA Object model, creating and using user defined objects.

Building forms, triggering subroutines by pressing a button on a form

Interacting with other applications with support for VBA, such as, SAP2000/ETABS or any other software used by civil engineers.

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-5

Using Python to manipulate Microsoft Excel files, creating, editing and saving Microsoft Excel files from Python, Interacting with Microsoft Excel using Python xl wings package, Calling Python from VBA.

Developing functions and subroutine for a comprehensive civil engineering application – RC design, Steel design, or other similar problems from other fields of Civil Engineering.

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Solve Trigonometric, Logarithmic, Exponential, Statistical problems and perform Matrix operations
2. Solve civil engineering problems using VB as a tool
3. Design structural elements by integrating excel and VB

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

Three Tests (preferably in MCQ pattern with 20 questions) each of 20 Marks (duration 01 hour)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of 10 Marks

1. First assignment at the end of 4th week of the semester
2. Second assignment at the end of 9th week of the semester

Quiz/Group discussion/Seminar, any two of three suitably planned to attain the COs and POs for 20 Marks (duration 01 hours)

1. The sum of total marks of three tests, two assignments, and quiz /seminar/ group discussion will be out of 100 marks and shall be scaled down to 50 marks

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of 01 mark. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is 01 hour. The student has to secure minimum of 35% of the maximum marks meant for SEE.

Suggested Learning Resources:
Books

1. Bourg, D.M., Excel Scientific and Engineering Cookbook, O'Reilly Media Inc., 2006.
2. Bilio, E.J., Excel for Scientists and Engineers – Numerical Methods, Wiley-Interscience, 2007.
3. Documentation for xlwingshttps://docs.xlwings.org/en/stable/

Web links and Video Lectures (e-Resources):

- https://freepdf-books.com/excel/
- https://jobscaptain.com/ms-excel-book-pdf/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Assignments to understand the operations in Excel and VB may be given to students

IIISemester

Personality Development and Soft skills (AEC)			
Course Code	**21CV383**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:0:0:0	SEE Marks	50
Total Hours of Pedagogy	15	Total Marks	100
Credits	1	Exam Hours	2

Course objectives: Enable the students to

1. Experience self-fulfilment and overall development of one's own personality by developing personal skills.
2. Develop awareness about the significance of soft skills and impactful personality in professional life.
3. Improve the soft skills like effective communication, business correspondence, impressive presentation, leadership qualities, team-work, Time management leading to successful performance in interviews and group discussions.
4. Identify opportunities in career building and enhancement with proper time management and stress management.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Chalk and talk
2. Power point Presentation, video
3. Group discussion
4. Enacting, Demonstration
5. Industry interaction

Module-1	
Introduction to Soft-Skills-Personal Skills: Knowing Oneself/Self-Discovery-Confidence Building-Defining Strengths- Developing Positive Attitude- Thinking Creatively-Improving Perceptions - Forming Values.	
Teaching-Learning Process	Chalk and talk, PowerPoint Presentation
Module-2	
Interpersonal and Social Skills: Understanding others-Developing Inter-personal relationship Team Building-Group dynamics-Networking-Problem-solving.	
Teaching-Learning Process	Chalk and talk, PowerPoint Presentation.
Module-3	
Communication Skills: Art of Listening-Art of Speaking-Art of Reading-Art of Writing-Art of Writing E-mails: Email etiquette	
Teaching-Learning Process	Chalk and talk, Enacting, Demonstration.
Module-4	
Presentation skills: Group discussion- mock Group Discussion using video recording - public speaking.	
Teaching-Learning Process	Chalk and talk, Enacting, Demonstration, Activity

Module-5	
Corporate Skills: Working with others- Developing a proper body language-behavioural etiquettes and mannerism- Time Management –Stress Management	
Teaching-Learning Process	Chalk and talk, PowerPoint Presentation

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

1. Develop effective communication skills (spoken and written) and effective presentation skills. Actively participate in group discussion / meetings / interviews and prepare & deliver presentations
2. Conduct effective business correspondence and prepare business reports which produce results.
3. Develop an understanding of and practice personal and professional responsibility.
4. Function effectively in multi-disciplinary and heterogeneous teams through the knowledge of team work, Inter-personal relationships, conflict management and leadership quality.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

Three Tests (preferably in MCQ pattern with 20 questions) each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

1. First assignment at the end of 4th week of the semester
2. Second assignment at the end of 9th week of the semester

Quiz/Group discussion/Seminar, any two of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

The sum of total marks of three tests, two assignments, and quiz /seminar/ group discussion will be out of 100 marks and shall be **scaled down to 50 marks**

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of 01 mark. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour.** The student has to secure minimum of 35% of the maximum marks meant for SEE.

Suggested Learning Resources:

Books

1. Meena K and V. Ayothi (2013) A Book on Development of Soft Skills (Soft Skills: A Road Map to Success), P. R. Publishers & Distributors, No. B-20 & 21, V. M. M Complex, Chatiram Bus Stand, Tiruchirappalli-620002. (Phone No: 0431-2702824Mobile No.: 9443370597, 9843074472)
2. Alex K. (2012) Soft Skills-Know Yourself & Know the World, S. Chand & Company LTD, Ram Nagar, New Delhi-110055. Mobile No.: 9442514814 (Dr.K.Alex

Web links and Video Lectures (e-Resources):

-

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Demonstrations of Videos
- Group Discussion
- Presentation on any social issues
- Quizzes

Semester III

Infrastructure Finance			
Course Code	21CV384	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:2:0:0	SEE Marks	50
Total Hours of Pedagogy	15	Total Marks	100
Credits	01	Exam Hours	1 hr

Course objectives:

- To understand the infrastructure components
- Opportunities in infrastructure development
- Financial sources and investment for infrastructure

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. The online courses available should be shared with students
2. YouTube videos
3. Power point presentations
4. Visit to government, public and private organizations to understand infrastructure projects planning and execution procedures

Module-1

An Introduction to Infrastructure Finance

What is Infrastructure Business? Infrastructure then and now, Sector Structure and Size, Estimating the per capita cost.

Models of the Infrastructure Sectors

Classification system, Infrastructure and Service Organization, Business Models of Infrastructure Subsystems, Matrix of Owners and users of Infrastructure systems

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-2

Infrastructure and services:

How Infrastructure systems serve the built environment, , Services Structures and Equipment, Infrastructure support sector.

Investor and Business Opportunities in Infrastructure

Introduction, Bond Market, Stocks of Infrastructure Companies, infrastructure Funds, Infrastructure Indices, Commodity markets, Mortgage-Backed Securities, Private Equity and Infrastructure, The Infrastructure Support Sector, Infrastructure Investment Media, Corruption in Infrastructure Business, International Spending Plans.

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-3

Infrastructure Performance

Tracking Infrastructure Performance, Systems to measure, Performance Standards, Infrastructure scorecard.

Financial Models for Infrastructure Organisations

General Management Model, General Financing Model, Sector Financing Models, Public Private Partnerships, Regulations.

Teaching-Learning	Chalk and talk, PowerPoint Presentation, YouTube videos

Process	

Module-4

Capital Markets for Infrastructure

Capital Requirement of Sectors, Capital flows of Infrastructure, Capital structure of Infrstructure sectors, Sources of Capital, Investment Banking.

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-5

Revenues for the Infrastructure Sectors

Flow of Revenues, Rate Regulation, Revenue and cost of service analysis, Infrastructure revenue by Sector.

Opportunities and Risks for Infrastructure

Infrastructure as a policy sector, Infrastructure Policy elements, Sector Issues, Transformational Issues.

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Prepare a comprehensive development plan for infrastructure projects
2. Plan funding required and procedure to be adopted for infrastructure development
3. Estimate revenue generation and implement investment plans
4. Understand risk involved and policy issues related to infrastructure projects

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

Three Tests (preferably in MCQ pattern with 20 questions) each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

1. First assignment at the end of 4th week of the semester
2. Second assignment at the end of 9th week of the semester

Quiz/Group discussion/Seminar, any two of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

The sum of total marks of three tests, two assignments, and quiz /seminar/ group discussion

will be out of 100 marks and shall be **scaled down to 50 marks**

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of 01 mark. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour.** The student has to secure minimum of 35% of the maximum marks meant for SEE.

Suggested Learning Resources:

Books

1. Infrastructure Finance, Dr. K B Singh, Dr. Ajay Pratap Yadav, ISBN: 9788195248070, First edition, 2021, Raj Publications
2. Project and Infrastructure Finance: Corporate Banking Perspective, Vikas Srivastava , V. Rajaraman, Oxford University press, ISBN-13 978-0199465002, 2017

Web links and Video Lectures (e-Resources):

- https://www.pdfdrive.com/project-finance-e40552174.html
- https://www.yumpu.com/en/document/view/63829168/e-book-download-principles-of-project-finance-full-free-collection

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Assignments on new planning and design of an infrastructure facility may be given

Semester III

Fire Safety in Buildings			
Course Code	21CV385	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:2:0:0	SEE Marks	50
Total Hours of Pedagogy	15	Total Marks	100
Credits	01	Exam Hours	1 hr

Course objectives:

- To understand the importance fire safety
- To learn various techniques involved in fire safety
- To design fire resistant buildings using proper materials and methods

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. The online courses available should be shared with students
2. YouTube videos
3. Power point presentations
4. Visit to fire stations and understand various fire accidents

Module-1

Fire: Introduction, Basic concepts of fire protection, Fire as a process of combustion, planning for fire protection, fire resistance

Ventilation and fuel controlled fire, process of combustion: flashover condition, effect of fire on construction material, design of fire resistance steel structure, concrete structure

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-2

Fire safety: urban planning, escape and refuge, internal planning, detection and suppression

Introduction to lift design, design of lift system, expected stop and floor of reversal, different cases, simulation, arrangements and escalators

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-3

Introduction to flow system: water supply, constant demand, variable demand and diversity factor, control systems

Flow in pipe networks and fixture units, design of water supply distribution system, flow in waste water pipes

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-4

Introduction to HVAC: governing equations to HVAC process, numerical problem on HVAC system, psychometric chart, equation based approach

Electrical systems: design of electrical systems, intelligent building, life cycle cost and basics of building maintenance, stages of maintenance management, planning for building maintenance, periodicity of maintenance management, estimation of repair cycle, cost profile of maintenance, lamp replacement, building inspection, planned and Ad-hoc maintenance

Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Module-5	
Condition survey and health evaluation of buildings, diagnosis of building by visual survey, case studies of visual survey, effect of corrosion and alkali aggregate reaction, sampling and choice of test location Non-destructive testing, core strength test, carbonation and chloride measurement, electrical method of progress measurement Repair, rehabilitation, retrofit, periodicity and economics of condition survey, interpretation of test results	
Teaching-Learning Process	Chalk and talk, PowerPoint Presentation, YouTube videos

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Understand types of fire, combustion process and fire resistance
2. Plan for fire safety and design of lifts
3. Design flow network in buildings
4. Design of electrical systems and maintenance
5. Perform health evaluation of buildings and suggest remedies

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

Three Tests (preferably in MCQ pattern with 20 questions) each of 20 Marks (duration 01 hour)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of 10 Marks

1. First assignment at the end of 4th week of the semester
2. Second assignment at the end of 9th week of the semester

Quiz/Group discussion/Seminar, any two of three suitably planned to attain the COs and POs for 20 Marks (duration 01 hours)

The sum of total marks of three tests, two assignments, and quiz /seminar/ group discussion will be out of 100 marks and shall be scaled down to 50 marks

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of 01 mark. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is 01 hour. The student has to secure minimum of 35% of the maximum marks meant for SEE.

Suggested Learning Resources:

Books

1. J A Purkiss, Fire Safety Engineering: Design of Structures, ISBN 13 978-8131220085, Elsevier, 2009
2. V K Jain, Fire Safety in Buildings, ISBN-13 978-938980219, New Age International Private Limited; Third edition, 2020
3. Fire protection, services and maintenance management of building, NPTEL video lecture, IIT, Delhi
4. Bureau of Indian Standards, " HAND BOOK OF FUNCTIONAL REQUIREMENTS OF BUILDINGS, (SP-41 & SP- 32)", BIS 1987 and 1989.
5. Markus,T.A. & Morris, E.N., "BUILDING CLIMATE AND ENERGY" Pitman publishing limited. 1980.
6. Croome,J.D.&Roberts,B.M.,"AIRCONDITIONING AND VENTILATION OF BUILDINGS VOL-1".Pergamon press.
7. Building Services Design - T.W.MEVER
8. Building Engineering & System Design - F.S.MERRIT & J. AMBROSE
9. SP-35 (1987): Handbook of Water supply & drainage-BIS
10. N.B.C.-2007 BIS
11. Concept of building fire safety - D.EGAN.
12. Design of fire resisting structures - H.L. MALHOTRA.

List of reference materials/books/

1. An introduction to fire dynamics -D.DRYSDALE
2. Structural fire protection Edt by T.T.LIE
3. Elevator technology - G.C.BARNEY
4. HEATING VENTILATING AND AIR CONDITIONING Analysis and Design - Faye C. McQuiston and Jerald D. Parker.
5. Building Maintenance Management-R.LEE
6. Developments In Building Maintenance -I.EJ. GIBSON
7. ConcreteStructures:materials,Maintenance And Repair D.CAMPBELL,ALLEN & H.ROPER

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/105/102/105102176/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Assignment students: A case study of fire hazard in building and restoration procedure adopted

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Computer Science and Engineering

Scheme of Teaching and Examinations2021

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

III SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21MAT31	Transform Calculus, Fourier Series and Numerical Techniques	Maths	3	0	0		03	50	50	100	3
2	IPCC 21CS32	Data Structures and Applications	Any CS Board Department	3	0	2		03	50	50	100	4
3	IPCC 21CS33	Analog and Digital Electronics		3	0	2		03	50	50	100	4
4	PCC 21CS34	Computer Organization and Architecture		3	0	0		03	50	50	100	3
5	PCC 21CSL35	Object Oriented Programming with JAVA Laboratory		0	0	2		03	50	50	100	1
6	UHV 21UH36	Social Connect and Responsibility	Any Department	0	0	1		01	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	TD and PSB: HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India and Professional Ethics										
8	AEC 21CS38X/21 CSL38X	Ability Enhancement Course - III	TD: Concerned department PSB: Concerned Board	If offered as Theory Course: 1	0	0		01	50	50	100	1
				If offered as lab. course: 0	0	2		02				
								Total	**400**	**400**	**800**	**18**

9	**Scheduled activities for III to VIII semesters**	NMDC 21NS83	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE) (Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out from (for 5 semesters) between III semester to VIII semester. SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the colander prepared for the NSS, PE and Yoga activities.
		NMDC 21PE83	Physical Education (PE) (Sports and Athletics)	PE	
		NMDC 21YO83	Yoga	Yoga	

Course prescribed to lateral entry Diploma holders admitted to III semester B.E./B.Tech programs

1	NCMC 21MATDIP31	Additional Mathematics - I	Maths	02	02	--	--	---	100	---	100	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course.
L –Lecture, **T –** Tutorial, P- Practical/ Drawing, **S –** Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination. **TD-**Teaching Department, **PSB**: Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and **21KBK37/47** Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical's of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

21INT49 Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internship of 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and has no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Ability Enhancement Course - III			
21CSL381	Mastering Office	21CS383	
21CS382	Programming IN c++	21CS384	

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Computer Science and Engineering

Scheme of Teaching and Examinations 2021

Outcome-Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

IV SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21CS41	Mathematical Foundations for Computing	Maths	2	2	0		03	50	50	100	3
2	IPCC 21CS42	Design and Analysis of Algorithms	Any CS Board Department	3	0	2		03	50	50	100	4
3	IPCC 21CS43	Microcontroller and Embedded SystemS		3	0	2		03	50	50	100	4
4	PCC 21CS44	Operating SystemS		2	2	0		03	50	50	100	3
5	AEC 21BE45	Biology For Engineers	BT, CHE, PHY	2	0	0		02	50	50	100	2
6	PCC 21CSL46	Python Programming Laboratory	Any CS Board Department	0	0	2		03	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India & Professional Ethics										
8	AEC 21CS48X/21CSL48X	Ability Enhancement Course- IV	TD and PSB: Concerned department	If offered as theory Course: 1	0	0		01	50	50	100	1
				If offered as lab. course: 0	0	2		02				
9	UHV 21UH49	Universal Human Values	Any Department	1	0	0		01	50	50	100	1
10	INT 21INT49	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period of II and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.				3	100	--	100	2
								Total	**550**	**450**	**1000**	**22**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

1	NCMC 21MATDIP41	Additional Mathematics - II	Maths	02	02	--	--	--	100	--	100	0

Note: BSC: Basic Science Course, IPCC: Integrated Professional Core Course, PCC: Professional Core Course, AEC –Ability Enhancement Courses, HSMC: Humanity and Social Science and Management Courses, UHV- Universal Human Value Courses.

L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical's of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from practical part of IPCC shall be included in the SEE question paper. For more details the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

Non – credit mandatory course (NCMC):

Additional Mathematics - II:

(1) Lateral entry Diploma holders admitted to III semester of B.E./B.Tech., shall attend the classes during the IV semester to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfil the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and has no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the course Additional Mathematics II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics II shall be indicated as Unsatisfactory.

Ability Enhancement Course - IV

21CSL481	Web Programming	21CSL483	R Programming
21CS482	Unix Shell Programming	21CS484	

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68 Innovation/ Entrepreneurship/ Societal based Internship.

(1) All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be considered under F (fail) grade and shall have to complete during subsequently after satisfying the internship requirements.

(2) Innovation/ Entrepreneurship Internship shall be carried out at industry, State and Central Government /Non-government organizations (NGOs), micro, small and medium enterprise (MSME), Innovation centers or Incubation centers. Innovation need not be a single major breakthrough; it can also be a series of small or incremental changes. Innovation of any kind can also happen outside of the business world.

Entrepreneurship internships offers a chance to gain hands on experience in the world of entrepreneurship and helps to learn what it takes to run a small entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business endeavours. Start-ups and small companies are a preferred place to learn the business tack ticks for future entrepreneurs as learning how a small business operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open the minds to creativity and innovation. Entrepreneurship internship can be from several sectors, including technology, small and medium-sized, and the service sector.

(3) Societal or social internship.

Urbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of many things that urban population enjoy. Rural internship, is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for better living.

As proposed under the AICTE rural internship programme, activities under Societal or social internship, particularly in rural areas, shall be considered for 40 points under AICTE activity point programme.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Computer Science and Engineering

Scheme of Teaching and Examinations 2021

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

V SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21CS51	Automata Theory and compiler Design	Any CS Board Department	3	0	0		03	50	50	100	3
2	IPCC 21CS52	Computer Networks		3	0	2		03	50	50	100	4
3	PCC 21CS53	Database Management Systems		3	0	0		03	50	50	100	3
4	PCC 21CS54	Artificial Intelligence and Machine Learning		3	0	0		03	50	50	100	3
5	PCC 21CSL55	Database Management Systems Laboratory with Mini Project		0	0	2		03	50	50	100	1
6	AEC 21XX56	Research Methodology & Intellectual Property Rights	TD: Any Department PSB: As identified by university	2	0	0		02	50	50	100	2
7	HSMC 21CIV57	Environmental Studies	TD: Civil/ Environmental /Chemistry/ Biotech. PSB: Civil Engg	1	0	0		1	50	50	100	1
8	AEC 21CS58X/21 CS58LX	Ability Enhancement Course-V	Concerned Board	If offered as Theory courses: 1	0	0		01	50	50	100	1
				If offered as lab. courses: 0	0	2		02				
								Total	**400**	**400**	**800**	**18**

Ability Enhancement Course - IV

21CSL581	Angular JS and Node JS	21CS583	
21CS582	C# and .Net Framework	21CS584	

Note: BSC: Basic Science Course, PCC: Professional Core Course, IPCC: Integrated Professional Core Course, AEC –Ability Enhancement Course INT – Internship, HSMC: Humanity and Social Science & Management Courses.
L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Integrated Professional Core Course (IPCC): refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). Theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by CIE only and there shall be no SEE. For more details the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Computer Science and Engineering

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(Effective from the academic year 2021 - 22)

VI SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	HSMC 21CS61	Software Engineering & Project Management	Any CS Board Department	2	2	0		03	50	50	100	3
2	IPCC 21CS62	Fullstack Development		3	0	2		03	50	50	100	4
3	PCC 21CS63	Computer Graphics and Fundamentals of Image Processing		3	0	0		03	50	50	100	3
4	PEC 21XX64x	Professional Elective Course-I		3	0	0		03	50	50	100	3
5	OEC 21XX65x	Open Elective Course-I	Concerned Department	3	0	0		03	50	50	100	3
6	PCC 21CSL66	Computer Graphics and Image Processing Laboratory	Any CS Board Department	0	0	2		03	50	50	100	1
7	MP 21CSMP67	Mini Project		Two contact hours /week for interaction between the faculty and students.				--	100	--	100	2
8	INT 21INT68	Innovation/Entrepreneurship /Societal Internship	Completed during the intervening period of IV and V semesters.					--	100	--	100	3
								Total	**500**	**300**	**800**	**22**

Professional Elective - I

21CS641	Agile Technology	21CS643	Advanced Computer Architecture
21CS642	Advanced JAVA Programming	21CS644	Data science and Visualization

Open Electives – I offered by the Department to other Department students

21CS651	Introduction to Data Structures	21CS653	Introduction to Cyber Security
21CS652	Introduction to Database Management Systems	21CS654	Programming in JAVA

Note: HSMC: Humanity and Social Science & Management Courses, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **PEC:** Professional Elective Courses, OEC–Open Elective Course, **MP** –Mini Project, INT –Internship.
L –Lecture, T – Tutorial, P - Practical / Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by CIE only and there shall be no SEE. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech) 2021-22 may be referred.

Professional Elective Courses (PEC):
A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course out of five courses. The minimum students' strength for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the programme is less than 10.

Open Elective Courses:
Students belonging to a particular stream of Engineering and Technology are not entitled for the open electives offered by their parent Department. However, they can opt an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor.
Selection of an open elective shall **not be allowed** if,

(i) The candidate has studied the same course during the previous semesters of the program.
(ii) The syllabus content of open electives is similar to that of the Departmental core courses or professional electives.
(iii) A similar course, under any category, is prescribed in the higher semesters of the program.

In case, any college is desirous of offering a course (not included in the Open Elective List of the University) from streams such as Law, Business

(MBA), Medicine, Arts, Commerce, etc., can seek permission, at least one month before the commencement of the semester, from the University by submitting a copy of the syllabus along with the details of expertise available to teach the same in the college.
The minimum students' strength for offering open electives is 10. However, this conditional shall not be applicable to cases where the admission to the programme is less than 10.

Mini-project work: Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications.
Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.
CIE procedure for Mini-project:
(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two faculty members of the Department, one of them being the Guide. The CIE marks awarded for the Mini-project work shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the project.
The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
No SEE component for Mini-Project.

VII semester Classwork and Research Internship /Industry Internship (21INT82)

Swapping Facility
Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate research internship/ industry internship after the VI semester**.**
(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the program.
Elucidation:
At the beginning of IV year of the programme i.e., after VI semester, VII semester classwork and VIII semester Research Internship /Industrial Internship shall be permitted to be operated simultaneously by the University so that students have ample opportunity for internship. In other words, a good percentage of the class shall attend VII semester classwork and similar percentage of others shall attend to Research Internship or Industrial Internship.
Research/Industrial Internship shall be carried out at an Industry, NGO, MSME, Innovation centre, Incubation centre, Start-up, Centers of Excellence (CoE), Study Centre established in the parent institute and /or at reputed research organizations / institutes. The internship can also be rural internship.
The mandatory Research internship /Industry internship is for 24 weeks. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during the subsequent University examination after satisfying the internship requirements.

INT21INT82 Research Internship/ Industry Internship/Rural Internship
Research internship: A research internship is intended to offer the flavour of current research going on in the research field. It helps students get familiarized with the field and imparts the skill required for carrying out research.
Industry internship: Is an extended period of work experience undertaken by students to supplement their degree for professional development. It also helps them learn to overcome unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with contingencies helps students recognize, appreciate, and adapt to organizational realities by tempering their knowledge with practical constraints.
Rural internship: A long-term goal, as proposed under the AICTE rural internship programme, shall be counted as rural internship activity.
The student can take up Interdisciplinary Research Internship or Industry Internship.
The faculty coordinator or mentor has to monitor the students' internship progress and interact with them to guide for the successful completion of the internship.
The students are permitted to carry out the internship anywhere in India or abroad. University shall not bear any expenses incurred in respect of internship.

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(Effective from the academic year 2021 - 22)

Swappable VII and VIII SEMESTER

VII SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	PCC 21CS71	Big Data Analytics	Any CS Board Department	3	0	0		3	50	50	100	3
2	PCC 21CS72	Cloud Computing		2	0	0		3	50	50	100	2
3	PEC 21XX73X	Professional elective Course-II		3	0	0		3	50	50	100	3
4	PEC 21XX74X	Professional elective Course-III		3	0	0		3	50	50	100	3
5	OEC 21XX75X	Open elective Course-II	Concerned Department	3	0	0		3	50	50	100	3
6	Project 21CSP76	Project work		Two contact hours /week for interaction between the faculty and students.				3	100	100	200	10
								Total	**350**	**350**	**700**	**24**

VIII SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	Seminar 21CS81		Technical Seminar		One contact hour /week for interaction between the faculty and students.				--	100	--	100	01
2	INT 21INT82		Research Internship/ Industry Internship		Two contact hours /week for interaction between the faculty and students.				03 (Batch wise)	100	100	200	15
3	NCMC	21NS83	National Service Scheme (NSS)	NSS	Completed during the intervening period of III semester to VIII semester.				--	50	50	100	0
		21PE83	Physical Education (PE) (Sports and Athletics)	PE									
		21YO83	Yoga	Yoga									
									Total	**250**	**150**	**400**	**16**

Professional Elective - II

21CS731	Object oriented Modelling and Design	21CS734	Blockchain Technology
21CS732	Digital Image Processing	21CS735	Internet of Things
21CS733	Cryptography and Network Security		

Professional Elective - III

21CS741	Software Architecture and Design Patterns	21CS744	Robotic Process Automation Design and Development
21CS742	Multiagent Systems	21CS745	NoSQL Data Base
21CS743	Deep Learning		

Open Electives - II offered by the Department to other Department students			
21CS751	Programming in Python	21CS754	Introduction to Data Science
21CS752	Introduction to AI and ML	21CS755	
21CS753	Introduction to Big Data		

Note: PCC: Professional Core Course, **PEC:** Professional Elective Courses, **OEC**–Open Elective Course, **AEC** –Ability Enhancement Courses.
L –Lecture, T – Tutorial, P- Practical / Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Note: VII and VIII semesters of IV year of the programme

(1) Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate research internship/ industry internship after the VI semester**.**

(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the programme.

PROJECT WORK (21XXP76): The objective of the Project work is

(i) To encourage independent learning and the innovative attitude of the students.
(ii) To develop interactive attitude, communication skills, organization, time management, and presentation skills.
(iii) To impart flexibility and adaptability.
(iv) To inspire team working.
(v) To expand intellectual capacity, credibility, judgment and intuition.
(vi) To adhere to punctuality, setting and meeting deadlines.
(vii) To instil responsibilities to oneself and others.
(viii) To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

CIE procedure for Project Work:

(1) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(2) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable. The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE procedure for Project Work: SEE for project work will be conducted by the two examiners appointed by the University. The SEE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25.

TECHNICAL SEMINAR (21XXS81): The objective of the seminar is to inculcate self-learning, present the seminar topic confidently, enhance communication skill, involve in group discussion for exchange of ideas. Each student, under the guidance of a Faculty, shall choose, preferably, a recent topic of his/her interest relevant to the programme of Specialization.

(i) Carry out literature survey, systematically organize the content.
(ii) Prepare the report with own sentences, avoiding a cut and paste act.
(iii) Type the matter to acquaint with the use of Micro-soft equation and drawing tools or any such facilities.
(iv) Present the seminar topic orally and/or through PowerPoint slides.
(v) Answer the queries and involve in debate/discussion.
(**vi)** Submit a typed report with a list of references.

The participants shall take part in the discussion to foster a friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Evaluation Procedure:

The CIE marks for the seminar shall be awarded (based on the relevance of the topic, presentation skill, participation in the question and answer session, and quality of report) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three teachers from the department with the senior-most acting as the Chairman.

Marks distribution for CIE of the course:

Seminar Report:50 marks
Presentation skill:25 marks
Question and Answer: 25 marks. ■ No SEE component for Technical Seminar

Non – credit mandatory courses (NCMC):

National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they has to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequently to earn the qualifying CIE marks subject to the maximum programme period.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

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III SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21MAT31	Mathematics Course (Common to all)	TD- Maths PSB-Maths					03	50	50	100	3
2	IPCC 21EC32	Digital System Design using Verilog	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
3	IPCC 21EC33	Basic Signal Processing	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
4	PCC 21EC34	Analog Electronic Circuits	TD: ECE PSB: ECE	3	0	0	1	03	50	50	100	3
5	PCC 21ECL35	Analog and Digital Electronics Lab	TD: ECE PSB: ECE	0	0	2		03	50	50	100	1
6	UHV 21UH36	Social Connect and Responsibility	Any Department	0	0	1		01	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	TD and PSB HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India and Professional Ethics										
8	AEC 21EC38X	Ability Enhancement Course - III	TD: Concerned department PSB: Concerned Board	If offered as Theory Course				01	50	50	100	1
				1	0	0						
				If offered as lab. course				02				
				0	0	2						
								Total	**400**	**400**	**800**	**18**

9	**Scheduled activities for III to VIII semesters**	NMDC 21NS83	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out between III semester to VIII semester (for 5 semesters). SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE and Yoga activities.
		NMDC 21PE83	Physical Education (PE)(Sports and Athletics)	PE	
		NMDC 21YO83	Yoga	Yoga	

Course prescribed to lateral entry Diploma holders admitted to III semester B.E./B.Tech programs

1	NCMC 21MATDIP31	Additional Mathematics - I	Maths	02	02	--	--	---	100	---	100	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course.
L –Lecture, **T –** Tutorial, P- Practical/ Drawing, **S –** Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD-**Teaching Department, **PSB**: Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and **21KBK37/47** Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

21INT49Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internship of 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Ability Enhancement Course - III			
21EC381	LD (Logic Design) Lab using Pspice / MultiSIM	21EC383	LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM
21EC382	AEC (Analog Electronic Circuits) Lab	21EC384	LabVIEW Programming Basics

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IV SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC **21EC41**	Maths for Communication Engineers	TD, PSB-Maths					03	50	50	100	3
2	IPCC 21EC42	Digital Signal Processing	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
3	IPCC 21EC43	Circuits & Controls	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
4	PCC 21EC44	Communication Theory	TD: ECE PSB: ECE	3	0	0	1	03	50	50	100	3
5	AEC 21BE45	Biology For Engineers	BT, CHE, PHY	2	0	0		02	50	50	100	2
6	PCC 21ECL46	Communication Laboratory I	TD: ECE PSB: ECE	0	0	2		03	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India & Professional Ethics										
8	AEC 21EC48X	Ability Enhancement Course- IV	TD and PSB: Concerned department	If offered as theory Course: 1	0	0		01	50	50	100	1
				If offered as lab. course: 0	0	2		02				
9	UHV 21UH49	Universal Human Values	Any Department	1	0	0		01	50	50	100	1
10	INT 21INT49	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period ofII and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.				3	100	--	100	2
								Total	**550**	**450**	**1000**	**22**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

1	NCMC 21MATDIP41	Additional Mathematics - II	Maths	02	02	--	--	--	100	--	100	0

Note: BSC: Basic Science Course, IPCC: Integrated Professional Core Course, PCC: Professional Core Course, AEC –Ability Enhancement Courses, HSMC: Humanity and Social Science and Management Courses, UHV- Universal Human Value Courses.
L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practicals of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from practical part of IPCCshall be included in the SEE question paper.For more details the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

Non – credit mandatory course (NCMC):

Additional Mathematics - II:

(1) Lateral entry Diploma holders admitted to III semester of B.E./B.Tech., shall attend the classes during the IV semester to complete all the

formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the course Additional Mathematics II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics II shall be indicated as Unsatisfactory.

Ability Enhancement Course - IV

21EC481	Embedded C Basics	21EC483	Octave / Scilab for Signals
21EC482	C++ Basics	21EC484	DAQ using LabVIEW

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68Innovation/ Entrepreneurship/ Societal based Internship.

(1) All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card.The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be considered under F (fail) grade and shall have to complete during subsequently after satisfying the internship requirements.

(2) Innovation/ Entrepreneurship Internship shall be carried out at industry, State and Central Government /Non-government organizations (NGOs), micro, small and medium enterprise (MSME), Innovation centres or Incubation centres. Innovation need not be a single major breakthrough; it can also be a series of small or incremental changes. Innovation of any kind can also happen outside of the business world.

Entrepreneurship internships offers a chance to gain hands on experience in the world of entrepreneurship and helps to learn what it takes to run a small entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business endeavours. Start-ups and small companies are a preferred place to learn the business tack ticks for future entrepreneurs as learning how a small business operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open the minds to creativity and innovation. Entrepreneurship internship can be from several sectors, including technology, small and medium-sized, and the service sector.

(3) Societal or social internship.

Urbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of many things that urban population enjoy. Rural internship is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for better living.

As proposed under the AICTE rural internship programme, activities under Societal or social internship, particularly in rural areas, shall be considered for 40 points under AICTE activity point programme.

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V SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self-Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21EC51	Digital Communication	TD: ECE PSB: ECE	3	0	0	1	03	50	50	100	3
2	IPCC 21EC52	Object Oriented Programming with Java & Data Structures	TD: ECE, CSE PSB: ECE	3	0	2		03	50	50	100	4
3	PCC 21EC53	Computer Communication Networks	TD: ECE PSB: ECE	3	0	0	1	03	50	50	100	3
4	PCC 21EC54	Microwave Theory & Antennas	TD: ECE PSB: ECE	3	0	0		03	50	50	100	3
5	PCC 21ECL55	Communication Lab II		0	0	2		03	50	50	100	1
6	AEC 21EC56	Research Methodology & Intellectual Property Rights	TD: Any Department PSB: As identified by University	2	0	0		02	50	50	100	2
7	HSMC 21CIV57	Environmental Studies	TD: Civil/ Environmental /Chemistry/ Biotech. PSB: Civil Engg	1	0	0		1	50	50	100	1
8	AEC 21EC58X	Ability Enhancement Course-V	Concerned Board	If offered as Theory courses: 1	0	0		01	50	50	100	1
				If offered as lab. courses: 0	0	2		02				
								Total	**400**	**400**	**800**	**18**

Ability Enhancement Course - V

21EC581	IoT (Internet of Things) Lab	21EC583	Antenna Design & Testing
21EC582	Communication Simulink Toolbox	21EC584	Microwaves toolbox

Note: BSC: Basic Science Course, PCC: Professional Core Course, IPCC: Integrated Professional Core Course, AEC –Ability Enhancement Course INT – Internship, HSMC: Humanity and Social Science & Management Courses.
L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Integrated Professional Core Course (IPCC): refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). Theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by CIE only and there shall be no SEE. For more details the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

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VI SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	HSMC 21EC61	Technological Innovation Management and Entrepreneurship	Any Department	3	0	0	0	03	50	50	100	3
2	IPCC 21EC62	Computer Organization & ARM Microcontrollers	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
3	PCC 21EC63	VLSI Design & Testing	TD: ECE PSB: ECE	3	0	0		03	50	50	100	3
4	PEC 21EC64x	Professional Elective Course-I	TD: ECE PSB: ECE					03	50	50	100	3
5	OEC 21EC65x	Open Elective Course-I	Concerned Department					03	50	50	100	3
6	PCC 21ECL66	VLSI Laboratory		0	0	2		03	50	50	100	1
7	MP 21ECMP67	Mini Project		Two contact hours /week for interaction between the faculty and students.				--	100	--	100	2
8	INT 21INT68	Innovation/Entrepreneurship /Societal Internship	Completed during the intervening period of IV and V semesters.					--	100	--	100	3
								Total	**500**	**300**	**800**	**22**

Professional Elective – I

21EC641	Artificial Neural Networks (L:T:P :: 2:2:0)	21EC643	Python Programming (L:T:P :: 2:0:2)
21EC642	Cryptography (L:T:P :: 2:2:0)	21EC644	Micro Electro Mechanical Systems (L:T:P :: 3:0:0)

Open Electives – I offered by the Department to other Department students

21EC651	Communication Engineering (L:T:P :: 3:0:0)	21EC653	Basic VLSI Design (L:T:P :: 3:0:0)
21EC652	Microcontrollers (L:T:P :: 3:0:0)	21EC654	Electronic Circuits with Verilog (L:T:P :: 2:0:2)
21EC655	Sensors & Actuators (L:T:P :: 3:0:0)		

Note: HSMC: Humanity and Social Science & Management Courses, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **PEC:** Professional Elective Courses, O**EC**–Open Elective Course, **MP** –Mini Project, INT –Internship.
L –Lecture, **T** – Tutorial, **P** - Practical / Drawing, **S** – Self Study Component, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Examination.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by CIE only and there shall be no SEE. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech) 2021-22 may be referred.

Professional Elective Courses(PEC):
A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course out of five courses. The minimum students' strength for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the programme is less than 10.

Open Elective Courses:
Students belonging to a particular stream of Engineering and Technology are not entitled for the open electives offered by their parent Department. However, they can opt an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor.
Selection of an open elective shall **not be allowed** if,

(i) The candidate has studied the same course during the previous semesters of the program.
(ii) The syllabus content of open electives is similar to that of the Departmental core courses or professional electives.
(iii) A similar course, under any category, is prescribed in the higher semesters of the program.

In case, any college is desirous of offering a course (not included in the Open Elective List of the University) from streams such as Law, Business

(MBA), Medicine, Arts, Commerce, etc., can seek permission, at least one month before the commencement of the semester, from the University by submitting a copy of the syllabus along with the details of expertise available to teach the same in the college.
The minimum students' strength for offering open electives is 10. However, this conditional shall not be applicable to cases where the admission to the programme is less than 10.

Mini-project work: Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications.
Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.
CIE procedure for Mini-project:
(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two faculty members of the Department, one of them being the Guide. The CIE marks awarded for the Mini-project work shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the project.
The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
No SEE component for Mini-Project.

VII semester Class work and Research Internship /Industry Internship (21INT82)

Swapping Facility
Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate research internship/ industry internship after the VI semester**.**
(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the program.
Elucidation:
At the beginning of IV year of the programme i.e., after VI semester, VII semester classwork and VIII semester Research Internship /Industrial Internship shall be permitted to be operated simultaneously by the University so that students have ample opportunity for internship. In other words, a good percentage of the class shall attend VII semester classwork and similar percentage of others shall attend to Research Internship or Industrial Internship.
Research/Industrial Internship shall be carried out at an Industry, NGO, MSME, Innovation centre, Incubation centre, Start-up, Centers of Excellence (CoE), Study Centre established in the parent institute and /or at reputed research organizations / institutes. The intership can also be rural internship.
The mandatory Research internship /Industry internship is for 24 weeks. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during the subsequent University examination after satisfying the internship requirements.

INT21INT82Research Internship/ Industry Internship/Rural Internship
Research internship: A research internship is intended to offer the flavour of current research going on in the research field. It helps students get familiarized with the field and imparts the skill required for carrying out research.
Industry internship: Is an extended period of work experience undertaken by students to supplement their degree for professional development. It also helps them learn to overcome unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with contingencies helps students recognize, appreciate, and adapt to organizational realities by tempering their knowledge with practical constraints.

The faculty coordinator or mentor has to monitor the students' internship progress and interact with them to guide for the successful completion of the internship.
The students are permitted to carry out the internship anywhere in India or abroad. University shall not bear any expenses incurred in respect of internship.

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Swappable VII and VIII SEMESTER

VII SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	PCC 21EC71	Advanced VLSI	TD: ECE PSB: ECE	3	0	0		3	50	50	100	3
2	PCC 21EC72	Optical & Wireless Communication	TD: ECE PSB: ECE	2	0	0		3	50	50	100	2
3	PEC 21EC72X	Professional elective Course-II	TD: ECE PSB: ECE					3	50	50	100	3
4	PEC 21EC73X	Professional elective Course-III	TD: ECE PSB: ECE					3	50	50	100	3
5	OEC 21EC74X	Open elective Course-II	Concerned Department					3	50	50	100	3
6	Project 21ECP75	Project work		Two contact hours /week for interaction between the faculty and students.				3	100	100	200	10
								Total	**350**	**350**	**700**	**24**

VIII SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	Seminar 21EC81		Technical Seminar		One contact hour /week for interaction between the faculty and students.				--	100	--	100	01
2	INT 21INT82		Research Internship/ Industry Internship		Two contact hours /week for interaction between the faculty and students.				03 (Batch wise)	100	100	200	15
3	NCMC	21NS83	National Service Scheme (NSS)	NSS	Completed during the intervening period of III semester to VIII semester.				--	50	50	100	0
		21PE83	Physical Education (PE) (Sports and Athletics)	PE									
		21YO83	Yoga	Yoga									
									Total	**250**	**150**	**400**	**16**

Professional Elective - II

21EC721	Advanced Design Tools for VLSI (L:T:P :: 2:0:2)	21EC724	Biomedical Signal Processing (L:T:P :: 3:0:0)
21EC722	Digital Image Processing (L:T:P :: 2:0:2)	21EC725	Speech Signal Processing (L:T:P :: 3:0:0)
21EC723	DSP Algorithms & Architecture (L:T:P :: 3:0:0)		

Professional Elective - III

21EC731	IoT & Wireless Sensor Networks (L:T:P :: 3:0:0)	21EC734	Machine Learning with Python (L:T:P :: 2:0:2)
21EC732	Network Security (L:T:P :: 3:0:0)	21EC735	Multimedia Communication (L:T:P :: 2:0:2)
21EC733	Fabrication technology (L:T:P :: 3:0:0)		

Open Electives - II offered by the Department to other Department students			
21EC741	Optical & Satellite Communication (L:T:P :: 3:0:0)	21EC744	Basic Digital Signal Processing (L:T:P :: 2:0:2)
21EC742	ARM Embedded Systems (L:T:P :: 3:0:0)	21EC745	E-waste Management (L:T:P :: 3:0:0)
21EC743	Basic Digital Image Processing (L:T:P :: 2:0:2)		

Note: PCC: Professional Core Course, **PEC:** Professional Elective Courses, **OEC**–Open Elective Course, **AEC** –Ability Enhancement Courses.
L –Lecture, T – Tutorial, P- Practical / Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Note: VII and VIII semesters of IV year of the programme

(1) Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate research internship/ industry internship after the VI semester**.**

(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the programme.

PROJECT WORK (21XXP75): The objective of the Project work is

(i) To encourage independent learning and the innovative attitude of the students.
(ii) To develop interactive attitude, communication skills, organization, time management, and presentation skills.
(iii) To impart flexibility and adaptability.
(iv) To inspire team working.
(v) To expand intellectual capacity, credibility, judgment and intuition.
(vi) To adhere to punctuality, setting and meeting deadlines.
(vii) To install responsibilities to oneself and others.
(viii) To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

CIE procedure for Project Work:

(1) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(2) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable. The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE procedure for Project Work: SEE for project work will be conducted by the two examiners appointed by the University. The SEE marks awarded for the project work shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25.

TECHNICAL SEMINAR (21XXS81): The objective of the seminar is to inculcate self-learning, present the seminar topic confidently, enhance communication skill, involve in group discussion for exchange of ideas. Each student, under the guidance of a Faculty, shall choose, preferably, a recent topic of his/her interest relevant to the programme of Specialization.

(i) Carry out literature survey, systematically organize the content.
(ii) Prepare the report with own sentences, avoiding a cut and paste act.
(iii) Type the matter to acquaint with the use of Micro-soft equation and drawing tools or any such facilities.
(iv) Present the seminar topic orally and/or through PowerPoint slides.
(v) Answer the queries and involve in debate/discussion.
(**vi)** Submit a typed report with a list of references.

The participants shall take part in the discussion to foster a friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Evaluation Procedure:

The CIE marks for the seminar shall be awarded (based on the relevance of the topic, presentation skill, participation in the question and answer session, and quality of report) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three teachers from the department with the senior-most acting as the Chairman.

Marks distribution for CIE of the course:

Seminar Report:50 marks
Presentation skill:25 marks
Question and Answer: 25 marks. ■No SEE component for Technical Seminar

Non – credit mandatory courses (NCMC):

National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they has to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequently to earn the qualifying CIE marks subject to the maximum programme period.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These course shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

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III Semester

Digital System Design Using Verilog			
Course Code	**21EC32**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

1. To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
2. To impart the concepts of designing and analyzing combinational logic circuits.
3. To impart design methods and analysis of sequential logic circuits.
4. To impart the concepts of Verilog HDL-data flow and behavioral models for the design of digital systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class .
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps- up to 4 variables, Quine-McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. (Section 3.1 to 3.5 of Text 1).

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-2

Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section 5.1 to 5.7 of Text 2)

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-3	
Flip-Flops and its Applications: The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, JK, D and SR flip-flops. (Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text 2)	
Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3
Module-4	
Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description. (Section 1.1 to 1.6.2, 1.6.4 (only Verilog), 2 of Text 3) **Verilog Data flow description:** Highlights of Data flow description, Structure of Data flow description. (Section 2.1 to 2.2 (only Verilog) of Text 3)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3
Module-5	
Verilog Behavioral description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (only Verilog) of Text 3) **Verilog Structural description**: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder. (Section 4.1 to 4.2 of Text 3)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Using suitable simulation software, demonstrate the operation of the following circuits:

Sl.No	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program.
2	To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description: 8:1 mux, 8:3 encoder, Priority encoder
6	To realize using Verilog Behavioral description: 1:8 Demux, 3:8 decoder, 2-bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a) JK type b) SR type c) T type and d) D type
8	To realize Counters - up/down (BCD and binary) using Verilog Behavioral description.
Demonstration Experiments (For CIE only – not to be included for SEE) Use FPGA/CPLD kits for downloading Verilog codes and check the output for interfacing experiments.	
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface a Relay or ADC to the FPGA/CPLD and demonstrate its working.
11	Verilog programs to interface DAC to the FPGA/CPLD for Waveform generation.
12	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

Course Outcomes

At the end of the course the student will be able to:

1. Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.
2. Analyze and design for combinational logic circuits.
3. Analyze the concepts of Flip Flops (SR, D, T and JK) and to design the synchronous sequential circuits using Flip Flops.
4. Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 will be scaled down to 50 marks.

Suggested Learning Resources:

Text Books

1. Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001.

2. Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.

3. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dreamtech press.

Reference Books:

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning

2. Logic Design, by Sudhakar Samuel, Pearson/ Sanguine, 2007

3. Fundamentals of HDL, by Cyril P R, Pearson/Sanguine 2010

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills.

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B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
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(Effective from the academic year 2021 – 22)

III Semester

Basic Signal Processing			
Course Code	**21EC33**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

Preparation: To prepare students with fundamental knowledge/ overview in the field of Signal Processing with Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications.

Core Competence: To equip students with a basic foundation of Signal Processing by delivering the basics of quantitative parameters for Matrices & Linear Transformations, the mathematical description of discrete time signals and systems, analyzing the signals in time domain using convolution sum, classifying signals into different categories based on their properties, analyzing Linear Time Invariant (LTI) systems in time and transform domains

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Vector Spaces: Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations Orthogonality: Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram-Schmidt Orthogonalization procedure

(Refer Chapters 2 and 3 of Text 1)

Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-2	
Eigen values and Eigen vectors: Review of Eigen values and Diagonalization of a Matrix, Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition. **(Refer Chapter 5, Text 1)**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3
Module-3	
Introduction and Classification of signals: Definition of signal and systems with examples, Elementary signals/Functions: Exponential, sinusoidal, step, impulse and ramp functions **Basic Operations on signals:** Amplitude scaling, addition, multiplication, time scaling, time shift and time reversal. Expression of triangular, rectangular and other waveforms in terms of elementary signals **System Classification and properties:** Linear-nonlinear, Time variant -invariant, causal-noncausal, static-dynamic, stable-unstable, invertible. **(Text 2) [Only for Discrete Signals & Systems]**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3
Module-4	
Time domain representation of LTI System: Impulse response, convolution sum. Computation of convolution sum using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular. **LTI system Properties in terms of impulse response:** System interconnection, Memory less, Causal, Stable, Invertible and Deconvolution and step response **(Text 2) [Only for Discrete Signals & Systems]**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3
Module-5	
The Z-Transforms: Z transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform by partial fraction, Causality and stability, Transform analysis of LTI systems. **(Text 2)**	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC	
Sl.No	**Experiments**
1	a. Program to create and modify a vector (array). b. Program to create and modify a matrix.
2	Programs on basic operations on matrix.
3	Program to solve system of linear equations.
4	Program for Gram-Schmidt orthogonalization.
5	Program to find Eigen value and Eigen vector.
6	Program to find Singular value decomposition.

7	Program to generate discrete waveforms.
8	Program to perform basic operation on signals.
9	Program to perform convolution of two given sequences.
10	a. Program to perform verification of commutative property of convolution. b. Program to perform verification of distributive property of convolution. c. Program to perform verification of associative property of convolution.
11	Program to compute step response from the given impulse response.
12	Programs to find Z-transform and inverse Z-transform of a sequence.

Course outcomes (Course Skill Set)

At the end of the course the student will be able to :

1. Understand the basics of Linear Algebra
2. Analyse different types of signals and systems
3. Analyse the properties of discrete-time signals & systems
4. Analyse discrete time signals & systems using Z transforms

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Programming assignment at the end of 9th week of the semester, which can be implemented using programming languages like C++/Python/Java/Scilab

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 will be scaled down to 50 marks.

Suggested Learning Resources:

Text Books

1. Gilbert Strang, "Linear Algebra and its Applications", Cengage Learning, 4th Edition, 2006, ISBN 97809802327
2. Simon Haykin and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN9971-51-239-4.

Reference Books:

1. **Michael Roberts,** "Fundamentals of Signals & Systems",2nd edition, Tata McGraw-Hill, 2010, ISBN978-0-07-070221-9.
2. **Alan** V **Oppenheim, Alan** S **WiIlsky and** S **Hamid Nawab,** "Signals and Systems" Pearson Education Asia / PHI, 2"" edition, 1997. Indian Reprint 2002.
3. **H P Hsu, R Ranjan,** "Signals and Systems", Schaum's outlines, TMH, 2006.
4. **B P Lathi,** "Linear Systems and Signals", Oxford University Press, 2005.
5. **Ganesh Rao and Satish Tunga,** "Signals and Systems", Pearson/Sanguine.
6. **Seymour Lipschutz, Marc Lipson**, "Schaums Easy Outline of Linear Algebra", 2020.

Web links and Video Lectures (e-Resources):

Video lectures on Signals and Systems by Alan V Oppenheim

Lecture 1, Introduction | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube

Lecture 2, Signals and Systems: Part 1 | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube

NPTEL video lectures signals and system:

https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx

Video lectures on Linear Algebra by Gilbert Strang

https://www.youtube.com/watch?v=ZK3O402wf1c&list=PL49CF3715CB9EF31D&index=1

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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III Semester

Analog Electronic Circuits			
Course Code	**21EC34**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to

- Explain various BJT parameters, connections and configurations.
- Design and demonstrate the diode circuits and transistor amplifiers.
- Explain various types of FET biasing and demonstrate the use of FET amplifiers.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1.Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2.Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4.Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5.Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6.Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7.Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor.

Small signal operation and Models: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model, The T model.

MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

[Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.7), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.7)]

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Basic BJT Amplifier Configurations- Design of Common Emitter and Common collector amplifier circuits. **RBT Level:** L1, L2, L3

Module-2

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower.

MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model.

Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low frequency response.

Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Discrete Circuit MOS Amplifier – The common source amplifier and the source follower. **RBT Level:** L1, L2, L3
Module-3	
Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). **Output Stages and Power Amplifiers:** Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Class D power amplifier. **RBT Level:** L1, L2, L3
Module-4	
Op-Amp Circuits: Op-amp DC and AC Amplifiers, DAC - Weighted resistor and R-2R ladder, ADC-Successive approximation type, Small Signal half wave rectifier, Absolute value output circuit, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. **555 Timer and its applications:** Monostable and Astable Multivibrators. [Text 2: 6.2, 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2,8.13 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Clippers and Clampers, Peak detector, Sample and hold circuit. **RBT Level:** L1, L2, L3
Module-5	
Overview of Power Electronic Systems: Power Electronic Systems, Power Electronic Converters and Applications. **Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-off Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A without design consideration. **Gate Trigger Circuit:** Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. [Text 3: 1.3, 1.5,1.6, 2.2,2.3,2.4,2.6, 2.7,2.9, 2.10,3.2,3.5.1, 3.5.2, 3.6.1, 3.6.3,3.6.4]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Basic Construction, working and applications of DIAC, TRIAC, IGBT, GTO. **RBT Level:** L1, L2, L3

Course Outcomes (Course Skill Set)

At the end of the course the student will be able to :

1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits.
2. Design and analyze FET amplifiers and oscillatorswith different circuit configurations and biasing conditions.
3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.
4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.
5. Understand the power electronic device components and its functions for basic power electronic circuits.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.

The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored out of 100 shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6thEdition, Oxford, 2015.ISBN:978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4thEdition, Pearson Education, 2018. ISBN: 978-93-325-4991-3
3. **MD Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897'**

Web links and Video Lectures (e-Resources):

- Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
- Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

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III Semester

Analog and Digital Electronics Lab			
Course Code	**21ECL35**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Study the static characteristics of SCR and test the RC triggering circuit.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

Sl.No.	**Experiments**
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator
3	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator
4	Obtain the static characteristics of SCR and test SCR Controlled HWR and FWR using RC triggering circuit.
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.
8	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192

9	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16
10	Pseudorandom sequence generator using IC7495
11	Test the precision rectifiers using opamp: i) Half wave rectifier ii) Full wave rectifier
12	Design and test Monostable and Astable Multivibrator using 555 Timer

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.
5. Demonstrate the basic electronic circuit experiments using SCR and 555 timer.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5th Edition, 2009, Oxford University Press.
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

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III Semester

LD (Logic Design) Lab using Pspice / MultiSIM			
Course Code	**21EC381**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Impart the concepts of De Morgan's Theorem, SOP, POS forms.
- Impart the concepts of designing and analyzing combinational logic circuits.
- Impart the concepts of analysis of sequential logic circuits.
- Analyze and design any given synchronous sequential circuits.

Sl.No	**Experiments**
1	Implementation of De Morgan's theorem and SOP/POS expressions using Pspice/Multisim.
2	Implementation of Half Adder, Full Adder, Half Subtractor and Full Subtractor using Pspice/ Multisim.
3	Design and implementation of 4-bit Parallel Adder/ Subtractor using IC 7483 and BCD to Excess-3 code conversion and vice-versa using Pspice/Multisim.
4	Design and implement of IC 7485 5-bit magnitude comparator using Pspice/Multisim.
5	To Realize Adder & Subtractor using IC 74153 (4:1 MUX) and 4-variable function using IC74151 (8:1MUX) using Pspice/Multisim.
6	To realize Adder and Subtractor using IC 74139/ 74155N (Demux/Decoder) and Binary to Gray code conversion & vice versa using 74139/ 74155N using Pspice/Multisim.
7	SR, Master-Slave JK, D & T flip-flops using NAND Gates using Pspice/Multisim.
8	Design and realize the Synchronous counters (up/down decade/binary) using Pspice/Multisim.
9	Realize the shift registers and their modes (SISO, PISO, PIPO, SIPO) using 7474/7495 using Pspice/Multisim.
10	Design Pseudo Random Sequence generator using 7495 using Pspice/Multisim.
11	Design Serial Adder with Accumulator and simulate using Pspice/Multisim.
12	Design using Pspice/Multisim Mod-N Counters.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the truth table of various expressions and combinational circuits using logic gates.
2. Design various combinational circuits such as adders, subtractors, comparators, multiplexers and code converters.
3. Construct flips-flops, counters and shift registers.
4. Design and implement synchronous counters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall

be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

- Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001
- Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.

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III Semester

AEC (Analog Electronic Circuits) Lab			
Course Code	21EC382	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	2

Course objectives:

- To provide practical exposure to the students on designing, setting up, executing and debugging various electronic circuits using simulation software.
- To give the knowledge and practical exposure on simple applications of analog electronic circuits.

Sl.No	**Experiments using Pspice/MultiSIM software**
1	Experiments to realize diode clipping (single, double ended) circuits.
2	Experiments to realize diode clamping (positive, negative) circuits.
3	Experiments to realize Full wave rectifier without filter (and set-up to measure the ripple factor, Vp-p, Vrms, etc.).
4	Design and conduct an experiment on Series Voltage Regulator using Zener diode to determine line/load regulation characteristics.
5	Realize BJT Darlington Emitter follower without bootstrapping and determine the gain, input and output impedances (other configurations of emitter follower can also be considered).
6	Set-up and study the working of complementary symmetry class B push pull power amplifier (other power amplifiers can also be suitably considered) and calculate the efficiency.
7	Design and set-up the oscillator circuits (Hartley, Colpitts, etc. using BJT/FET) and determine the frequency of oscillation.
8	Design and set-up the crystal oscillator and determine the frequency of oscillation.
9	Experiment to realize Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.
10	Experiments to realize Transfer and drain characteristics of a MOSFET.
11	Experiments to realize UJT triggering circuit for Controlled Full wave Rectifier.
12	Design and simulation of Regulated power supply.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Understand the circuit schematic and its working.
2. Study the characteristics of different electronic devices.
3. Design and test simple electronic circuits as per the specifications using discrete electronic components.
4. Compute the parameters from the characteristics of active devices.
5. Familiarize with EDA software which can be used for electronic circuit simulation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book.

Suggested Learning Resources:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.
2. Muhammed H Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", 3rd Edition, Prentice Hall, 2003.

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III Semester

LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM			
Course Code	**21EC383**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- To apply operational amplifiers in linear and nonlinear applications.
- To acquire the basic knowledge of special function ICs.
- To use Multisim/Pspice software for circuit design and simulation

Sl.No	**Experiments using Pspice / MultiSIM** Every experiment has to be designed, circuit to be drawn / constructed and executed in the specified software. Results are also to be noted and inferred.
	Note: Standard design procedure to be adopted.
1	To realize using op-amp an Inverting Amplifier and Non-Inverting Amplifier
2	To realize using op-amps i) Summing Amplifier ii)Difference amplifier
3	To realize using op-amps an Instrumentation Amplifier
4	To realize using op-amps i) Differentiator ii)Integrator
5	To realize using op-amps a Full wave Precision Rectifier
6	To realize using op-amps • Inverting and Non-Inverting Zero Crossing Detectors • Positive and Negative Voltage level detectors
7	To realize using op-amp an Inverting Schmitt Trigger
8	To realize using op-amp an Astable Multivibrator
9	To design and implement using op-amps • Butterworth I & II order Low Pass Filter • Butterworth I & II order High Pass Filter
10	To design and implement using op-amp a RC Phase Shift Oscillator
11	To design and implement Mono-stable Multivibrator using 555 timer
12	To design and implement 4 - bit R-2R Digital to Analog Converter

Course outcomes (Course Skill Set):

After studying this course, students will be able to;

1. Sketch/draw circuit schematics, construct circuits, analyze and troubleshoot circuits containing op-amps, resistors, diodes, capacitors and independent sources.
2. Relate to the manufacturer's data sheets of IC 555 timer and IC µa741 op-amp.
3. Realize and verify the operation of analog integrated circuits like Amplifiers, Precision Rectifiers, Comparators and Waveform generators.
4. Design and implement analog integrated circuits like Oscillators, Active filters, Timer circuits, Data converters and compare the experimental results with theoretical values.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018.

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III Semester

LabVIEW Programming Basics			
Course Code	**21EC384**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Aware of various front panel controls and indicators.
- Connect and manipulate nodes and wires in the block diagram.
- Locate various toolbars and pull-down menus for the purpose of implementing specific functions.
- Locate and utilize the context help window.
- Familiar with LabVIEW and different applications using it.
- Run a Virtual Instrument (VI).

Sl.No	**VI Programs (using LabVIEW software) to realize the following:**
1	Basic arithmetic operations: addition, subtraction, multiplication and division
2	Boolean operations: AND, OR, XOR, NOT and NAND
3	Sum of 'n' numbers using 'for' loop
4	Factorial of a given number using 'for' loop
5	Determine square of a given number
6	Factorial of a given number using 'while 'loop
7	Sorting even numbers using 'while' loop in an array
8	Finding the array maximum and array minimum
	Demonstration Experiments (For CIE)
9	Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically.
10	Build a Virtual Instrument that simulates a Basic Calculator (using formula node).
11	Build a Virtual Instrument that simulates a Water Level Detector.
12	Demonstrate how to create a basic VI which calculates the area and perimeter of a circle.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Use Lab VIEW to create data acquisition, analysis and display operations
2. Create user interfaces with charts, graph and buttons
3. Use the programming structures and data types that exist in Lab VIEW
4. Use various editing and debugging techniques

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI, 2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw Hill, Second Edition, 2011.

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IV Semester

Maths for Communication Engineers			
Course Code	**21EC41**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

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IV Semester

Digital Signal Processing			
Course Code	21EC42	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives:

1. **Preparation:** To prepare students with fundamental knowledge/ overview in the field of Digital Signal Processing
2. **Core Competence:** To equip students with a basic foundation of Signal Processing by delivering the basics of Discrete Fourier Transforms & their properties, design of filters and overview of digital signal processors

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes
10. Give Programming Assignments

Module-1

Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution **[Text 1]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-2

Additional DFT Properties, **Linear filtering methods based on the DFT:** Use of DFT in Linear Filtering, Filtering of Long data Sequences. Fast-Fourier-Transform (FFT) algorithms: Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT decimation in-time **[Text 1]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-3

Design of FIR Filters: Characteristics of practical frequency-selective filters, Symmetric and Anti-symmetric FIR filters, Design of Linear-phase FIR (low pass and High pass) filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Structure for FIR Systems: Direct form, Cascade form and Lattice structures **[Text1]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-4

IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Low pass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth (Lowpass and Highpass) Filter Design using BLT. Realization of IIR Filters in Direct form I and II **[Text 2]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

Module-5

Digital Signal Processors: DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, FIR and IIR filter implementations in Fixed point systems. **[Text 2]**

Teaching-Learning Process	Chalk and Talk, YouTube videos, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

List of Programs to be implemented & executed using any programming languages like C++/Python/Java/Scilab / MATLAB/CC Studio (but not limited to)

1. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.
2. Computation of circular convolution of two given sequences and verification of commutative, distributive and associative property of convolution.
3. Computation of linear convolution of two sequences using DFT and IDFT.
4. Computation of circular convolution of two given sequences using DFT and IDFT
5. Verification of Linearity property, circular time shift property & circular frequency shift property of DFT.
6. Verification of Parseval's theorem
7. Design and implementation of IIR (Butterworth) low pass filter to meet given specifications.
8. Design and implementation of IIR (Butterworth) high pass filter to meet given specifications.
9. Design and implementation of low pass FIR filter to meet given specifications.
10. Design and implementation of high pass FIR filter to meet given specifications.
11. To compute N- Point DFT of a given sequence using DSK 6713 simulator
12. To compute linear convolution of two given sequences using DSK 6713 simulator
13. To compute circular convolution of two given sequences using DSK 6713 simulator

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Determine response of LTI systems using time domain and DFT techniques
2. Compute DFT of real and complex discrete time signals
3. Compute DFT using FFT algorithms
4. Design FIR and IIR Digital Filters
5. Design of Digital Filters using DSP processor

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Programming assignment at the end of 9th week of the semester, which can be implemented using programming languages like C++/Python/Java/Scilab

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

Suggested Learning Resources:

Text Books:

1. Proakis & Manolakis, “Digital Signal Processing - Principles Algorithms & Applications”, 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2. Li Tan, Jean Jiang, “Digital Signal processing - Fundamentals and Applications”, Academic Press, 2013, ISBN: 978-0-12-415893.

Reference Books:

1. Sanjit K Mitra, “Digital Signal Processing, A Computer Based Approach”, 4th Edition, McGraw Hill Education, 2013,
2. Oppenheim & Schaffer, “Discrete Time Signal Processing", PHI, 2003.
3. D Ganesh Rao and Vineeth P Gejji, “Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

Web links and Video Lectures (e-Resources):

By Prof. S. C. Dutta Roy, IIT Delhi

https://nptel.ac.in/courses/117102060

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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IV Semester

Circuits & Controls			
Course Code	**21EC43**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

1. Apply mesh and nodal techniques to solve an electrical network.
2. Solve different problems related to Electrical circuits using Network Theorems and Two port network.
3. Familiarize with the use of Laplace transforms to solve network problems.
4. Understand basics of control systems and design mathematical models using block diagram reduction, SFG, etc.
5. Understand Time domain and Frequency domain analysis.
6. Familiarize with the State Space Model of the system.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class .
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Basic concepts and network theorems

Types of Sources, Loop analysis, Nodal analysis with independent DC and AC Excitations.
(Textbook 1: 2.3, 4.1, 4.2, 4.3, 4.4, 10.6)

Super position theorem, Thevenin's theorem, Norton's Theorem, Maximum Power transfer Theorem.
(Textbook 2: 9.2, 9.4, 9.5, 9.7)

Teaching-Learning Process	Chalk and Talk, YouTube videos, Demonstrate the concepts using circuits **RBT Level:** L1, L2, L3

Module-2	
Two port networks: Short- circuit Admittance parameters, Open- circuit Impedance parameters, Transmission parameters, Hybrid parameters (Textbook 3: 11.1, 11.2, 11.3, 11.4, 11.5) **Laplace transform and its Applications**: Step Ramp, Impulse, Solution of networks using Laplace transform, Initial value and final value theorem (Textbook 3: 7.1, 7.2, 7.4, 7.7, 8.4)	
Teaching-Learning Process	Chalk and Talk **RBT Level:** L1, L2, L3
Module-3	
Basic Concepts and representation: Types of control systems, effect of feedback systems, differential equation of physical systems (only electrical systems), Introduction to block diagrams, transfer functions, Signal Flow Graphs (Textbook 4: Chapter 1.1, 2.2, 2.4, 2.5, 2.6)	
Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3
Module-4	
Time Response analysis: Time response of first order systems. Time response of second order systems, time response specifications of second order systems (Textbook 4: Chapter 5.3, 5.4) **Stability Analysis:** Concepts of stability necessary condition for stability, Routh stability criterion, relative stability Analysis (Textbook 4: Chapter 5.3, 5.4, 6.1, 6.2, 6.4, 6.5)	
Teaching-Learning Process	Chalk and Talk, Any software tool to show time response **RBT Level:** L1, L2, L3
Module-5	
Root locus: Introduction the root locus concepts, construction of root loci (Textbook 4: 7.1, 7.2, 7.3) **Frequency Domain analysis and stability**: Correlation between time and frequency response and Bode plots (Textbook 4: 8.1, 8.2, 8.4) **State Variable Analysis:** Introduction to state variable analysis: Concepts of state, state variable and state models. State model for Linear continuous –Time systems, solution of state equations. (Textbook 4: 12.2, 12.3, 12.6)	
Teaching-Learning Process	Chalk and Talk, Any software tool to plot Root locus, Bode plot **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Using suitable hardware and simulation software, demonstrate the operation of the following circuits:

Sl.No	Experiments
1	Verification of Superposition theorem
2	Verification of Thevenin's theorem
3	Speed torque characteristics of i)AC Servomotor ii) DC Servomotors
4	Determination of time response specification of a second order Under damped System, for different damping factors.
5	Determination of frequency response of a second order System
6	Determination of frequency response of a lead lag compensator
7	Using Suitable simulation package study of speed control of DC motor using i) Armature control ii) Field control

8	Using suitable simulation package, draw Root locus & Bode plot of the given transfer function.
Demonstration Experiments (For CIE only, not for SEE)	
9	Using suitable simulation package, obtain the time response from state model of a system.
10	Implementation of PI, PD Controllers.
11	Implement a PID Controller and hence realize an Error Detector.
12	Demonstrate the effect of PI, PD and PID controller on the system response.

Course Outcomes

At the end of the course the student will be able to:

1. Analyse and solve Electric circuit, by applying, loop analysis, Nodal analysis and by applying network Theorems.
2. Evaluate two port parameters of a network and Apply Laplace transforms to solve electric networks.
3. Deduce transfer function of a given physical system, from differential equation representation or Block Diagram representation and SFG representation.
4. Calculate time response specifications and analyse the stability of the system.
5. Draw and analyse the effect of gain on system behaviour using root loci.
6. Perform frequency response Analysis and find the stability of the system.
7. Represent State model of the system and find the time response of the system.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and

scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 shall be reduced proportionally to 50.

Suggested Learning Resources:

Text Books

1. Engineering circuit analysis, William H Hayt, Jr, Jack E Kemmerly, Steven M Durbin, Mc Graw Hill Education, Indian Edition 8e.
2. Networks and Systems, D Roy Choudhury, New age international Publishers, second edition.
3. Network Analysis, M E Van Valkenburg, Pearson, 3e.
4. Control Systems Engineering, I J Nagrath, M. Gopal, New age international Publishers, Fifth edition.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/108106098
- https://nptel.ac.in/courses/108102042

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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IV Semester

Communication Theory			
Course Code	**21EC44**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM., Low pass sampling and Quantization as a random process.
- Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
- Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
- Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector.

DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION: Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing.

SINGLE SIDE–BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION: SSB Modulation, VSB Modulation, Frequency Translation, Frequency Division Multiplexing, Theme Example: VSB Transmission of Analog and Digital Television.

[Text1: 3.1 to 3.8]

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Properties of the Fourier Transform, Dirac Delta Function. **RBT Level:** L1, L2, L3

Module-2

ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase–Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM

Systems. The Superheterodyne Receiver [Text1: 4.1 to 4.6]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** FM Broadcasting System [Ref1] **RBT Level:** L1, L2, L3
Module-3	
NOISE: Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth. **NOISE IN ANALOG MODULATION**: Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Preemphasis and De-emphasis in FM (Text1: 5.10, 6.1 to 6.6)	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** Mean, Correlation and Covariance functions of Random Processes **RBT Level:** L1, L2, L3
Module-4	
SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources? The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. (Text1: 7.1 to 7.7)	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** T1 carrier systems [Ref1] **RBT Level:** L1, L2, L3
Module-5	
SAMPLING AND QUANTIZATION (Contd): The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation (Text1: 7.8 to 7.10), Application examples - (a) Video + MPEG (Text1:7.11) and (b) Vocoders (refer Section 6.8 of Reference Book 1)	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos. **Self-study topics:** Digital Multiplexing. [Ref1] **RBT Level:** L1, L2, L3

Course Outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the amplitude and frequency modulation techniques and perform time and frequency domain transformations.
2. Identify the schemes for amplitude and frequency modulation and demodulation of analog signals and compare the performance.
3. Characterize the influence of channel noise on analog modulated signals.
4. Understand the characteristics of pulse amplitude modulation, pulse position modulation and pulse code modulation systems.
5. Illustration of digital formatting representations used for Multiplexers, Vocoders and Video transmission.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Simon Haykins & Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books

1. B P Lathi and Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press., 4th edition, 2010, ISBN: 97801980738002.
2. Simon Haykins, An Introduction to Analog and Digital Communication, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. H Taub & D L Schilling, Principles of Communication Systems, TMH, 2011.

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IV Semester

Communication Laboratory I			
Course Code	**21ECL46**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Model an analog communication system signal transmission and reception.
- Realize the electronic circuits to perform analog and pulse modulations and demodulations.
- Verify the sampling theorem and relate the signal and its spectrum before and after sampling.
- Understand the process of PCM and delta modulations.
- Understand the PLL operation.

Sl.No.	**Experiments**
1	Design of active second order Butterworth low pass and high pass filters.
2	Amplitude Modulation and Demodulation of (a) Standard AM and (b) DSBSC (LM741 and LF398 ICs can be used)
3	Frequency modulation and demodulation
4	Design and test Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5	Design and test i) Pulse sampling, flat top sampling and reconstruction. ii) Pulse amplitude modulation and demodulation.
6	Design and test BJT/FET Mixer
7	Pulse Code Modulation and demodulation
8	Phase locked loop Synthesis
9	Illustration of (a) AM modulation and demodulation and display the signal and its spectrum. (b) DSB-SC modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)
10	Illustration of FM modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)
11	Illustrate the process of sampling and reconstruction of low pass signals. Display the signals and its spectrums of both analog and sampled signals. (Use MATLAB/SCILAB).
12	Illustration of Delta Modulation and the effects of step size selection in the design of DM encoder. (Use MATLAB/SCILAB)

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the AM and FM modulation and demodulation by representing the signals in time and frequency domain.
2. Design and test the sampling, Multiplexing and PAM with relevant circuits.
3. Demonstrate the basic circuitry and operations used in AM and FM receivers.
4. Illustrate the operation of PCM and delta modulations for different input conditions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by

examiners.
General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Louis E Frenzel, Principles of Electronic Communication Systems, McGraw Hill Education (India) Private Limited, 2016.
2. B P Lathi, Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press, 2015.

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IV Semester

Embedded C Basics			
Course Code	**21EC481**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

- Understand the basic programming of Microprocessor and microcontroller.
- To develop the microcontroller-based programs for various applications.

Sl.No	**Experiments**
	Conduct the following experiments by writing C Program using Keil microvision simulator (any 8051 microcontroller can be chosen as the target).
1	Write a 8051 C program to multiply two 16 bit binary numbers.
2	Write a 8051 C program to find the sum of first 10 integer numbers.
3	Write a 8051 C program to find factorial of a given number.
4	Write a 8051 C program to add an array of 16 bit numbers and store the 32 bit result in internal RAM
5	Write a 8051 C program to find the square of a number (1 to 10) using look-up table.
6	Write a 8051 C program to find the largest/smallest number in an array of 32 numbers
7	Write a 8051 C program to arrange a series of 32 bit numbers in ascending/descending order
8	Write a 8051 C program to count the number of ones and zeros in two consecutive memory locations.
9	Write a 8051 C program to scan a series of 32 bit numbers to find how many are negative.
10	Write a 8051 C program to display “Hello World” message (either in simulation mode or interface an LCD display).
11	Write a 8051 C program to convert the hexadecimal data 0xCFh to decimal and display the digits on ports P0, P1 and P2 (port window in simulator).

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Write C programs in 8051 for solving simple problems that manipulate input data using different instructions of 8051 C.
2. Develop testing and experimental procedures on 8051 Microcontroller, analyze their operation under different cases.
3. Develop programs for 8051 Microcontroller to implement real world problems.
4. Design and Develop Mini projects

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.
The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.
Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
Weightage to be given for neatness and submission of record/write-up on time.
Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).
The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.
SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University
All laboratory experiments are to be included for practical examination.
(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours
Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

"The 8051 Microcontroller: Hardware, Software and Applications", V Udayashankara and M S Mallikarjuna Swamy, McGraw Hill Education, 1st edition, 2017.

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IV Semester

C++ Basics			
Course Code	**21EC482**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Understand object-oriented programming concepts, and apply them in solving problems.
- To create, debug and run simple C++ programs.
- Introduce the concepts of functions, friend functions, inheritance, polymorphism and function overloading.
- Introduce the concepts of exception handling and multithreading.

Sl.No	**Experiments**
1	Write a C++ program to find largest, smallest & second largest of three numbers using inline functions MAX & Min.
2	Write a C++ program to calculate the volume of different geometric shapes like cube, cylinder and sphere using function overloading concept.
3	Define a STUDENT class with USN, Name & Marks in 3 tests of a subject. Declare an array of 10 STUDENT objects. Using appropriate functions, find the average of the two better marks for each student. Print the USN, Name & the average marks of all the students.
4	Write a C++ program to create class called MATRIX using two-dimensional array of integers, by overloading the operator == which checks the compatibility of two matrices to be added and subtracted. Perform the addition and subtraction by overloading + and – operators respectively. Display the results by overloading the operator <<. If (m1 == m2) then m3 = m1 + m2 and m4 = m1 – m2 else display error
5	Demonstrate simple inheritance concept by creating a base class FATHER with data members: *First Name, Surname, DOB & bank Balance* and creating a derived class SON, which inherits: Surname & Bank Balance feature from base class but provides its own feature: First Name & DOB. Create & initialize F1 & S1 objects with appropriate constructors & display the FATHER & SON details.
6	Write a C++ program to define class name FATHER & SON that holds the income respectively. Calculate & display total income of a family using Friend function.
7	Write a C++ program to accept the student detail such as name & 3 different marks by get_data() method & display the name & average of marks using display() method. Define a friend function for calculating the average marks using the method mark_avg().
8	Write a C++ program to explain virtual function (Polymorphism) by creating a base class polygon which has virtual function areas two classes rectangle & triangle derived from polygon & they have area to calculate & return the area of rectangle & triangle respectively.
9	Design, develop and execute a program in C++ based on the following requirements: An EMPLOYEE class containing data members & members functions: i) Data members: employee number (an integer), Employee_ Name (a string of characters), Basic_ Salary (in integer), All_ Allowances (an integer), Net_Salary (an integer). (ii) Member functions: To read the data of an employee, to calculate Net_Salary & to print the values of all the data members. (All_Allowances = 123% of Basic, Income Tax (IT) =30% of gross salary (=basic_ Salary_All_Allowances_IT).
10	Write a C++ program with different class related through multiple inheritance & demonstrate the use of different access specified by means of members variables & members functions.
11	Write a C++ program to create three objects for a class named count object with data members

	such as roll_no & Name. Create a members function set_data ( ) for setting the data values & display ( ) member function to display which object has invoked it using „this" pointer.
12	Write a C++ program to implement exception handling with minimum 5 exceptions classes including two built in exceptions.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Write C++ program to solve simple and complex problems
2. Apply and implement major object-oriented concepts like message passing, function overloading, operator overloading and inheritance to solve real-world problems.
3. Use major C++ features such as Templates for data type independent designs and File I/O to deal with large data set.
4. Analyze, design and develop solutions to real-world problems applying OOP concepts of C++

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and

result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Object oriented programming in TURBO C++, Robert Lafore, Galgotia Publications, 2002
2. The Complete Reference C++, Herbert Schildt, 4th Edition, Tata McGraw Hill, 2003.
3. Object Oriented Programming with C++, E Balaguruswamy, 4th Edition, Tata McGraw Hill, 2006.

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IV Semester

Octave / Scilab for Signals			
Course Code	**21EC483**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

1. **Preparation**: To prepare students with fundamental knowledge/ overview in the field of signals and processing.
2. **Core Competence**: To equip students with a basic foundation in electronic engineering and mathematics fundamentals required for comprehending the operation and application of signal processing.
3. **Professionalism & Learning Environment**: To inculcate in students an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.

Sl.No	**Experiments**
1	Verify the Sampling theorem.
2	Determine linear convolution, Circular convolution and Correlation of two given sequences. Verify the result using theoretical computations.
3	Determine the linear convolution of two given point sequences using FFT algorithm. Verify the result using theoretical computations.
4	Determine the correlation using FFT algorithm. Verify the result using theoretical computations.
5	Determine the spectrum of the given sequence using FFT. Verify the result using theoretical computations.
6	Design and test FIR filter using Windowing method (Hamming, Hanning and Rectangular window) for the given order and cut-off frequency.
7	Design and test IIR Butterworth 1^{st} and 2^{nd} order low & high pass filter.
8	Design and test IIR Chebyshev 1^{st} and 2^{nd} order low & high pass filter.
9	Generation of an AM – Suppressed Carrier Wave & visualization of the time domain and frequency domain plots.
10	Generation and visualization of standard test signals (both continuous and discrete time).
11	Generation and visualization of audio signal (pre-recorded) and generation of echo.
12	Generation and visualization of the STFT of a chirp (and other related) signal.

Course outcomes (Course Skill Set):
At the end of the course the student will be able to:

- Demonstrate the DSP concepts on signal generation and sampling using Scilab/Octave
- Design and verify the computation of discrete signals using Scilab/Octave.
- Demonstrate and verify the application of FFT/DFT algorithm for a given signal using Scilab/Octave.
- Design and demonstrate programs to evaluate different types of low and high pass FIR filters using Scilab/Octave.
- Design, demonstrate and visualize different real world signals using Scilab/Octave programs.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.

Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).

Weightage to be given for neatness and submission of record/write-up on time.

Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.

In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book

The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

Digital Signal Processing Using MATLAB, John G Proakis and Vinay K Ingle, Cengage Learning, 2011

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IV Semester

DAQ using LabVIEW			
Course Code	21EC484	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Process the knowledge of loop constructs.
- Fundamentals of graphical programming and use LabVIEW modules
- Implement 'Timing' functions.
- Input algebraic formulas via 'Formula Nodes' and 'Expression Nodes'.

Sl.No	**Experiments**
1	Data acquisition using LabVIEW for temperature measurement with thermocouple.
2	Data acquisition using LabVIEW for temperature measurement with AD590.
3	Data acquisition using LabVIEW for temperature measurement with RTD.
4	Data acquisition using LabVIEW for temperature measurement with Thermistor.
5	Creation of a CRO using LabVIEW and measurement of frequency and amplitude from external source.
6	Create function generator using LabVIEW and display the amplitude and frequency on CRO (externally connected)
7	Demonstrate amplitude modulation considering modulating and carrier wave from external source.
8	Interface LEDs to DAQ output and implement counter.
9	Data acquisition using LabVIEW for load / strain measurement using suitable transducers.
10	Demonstrate binary to grey code converter (& vice versa) using DAQ card.
11	Data acquisition using LabVIEW for distance/humidity measurement using suitable transducers.
12	Reading audio input with Microphones and output using DAQ card.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Build temperature indicating instruments using LabVIEW (NI DAQ)
2. Interface peripheral devices/instruments to LabVIEW
3. Build LabVIEW modules to sense and process audio inputs
4. Apply programming structures, data types, and the analysis and signal processing algorithms in LabVIEW
5. Debug and troubleshoot applications

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
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- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
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- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI, 2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw Hill, Second Edition, 2011.

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V Semester

Digital Communication			
Course Code	**21EC51**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
- Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
- Understand the principles of spread spectrum communications.
- Understand the basic principles of information theory and various source coding techniques.
- Build a comprehensive knowledge about various Source and Channel Coding techniques.
- Discuss the different types of errors and error detection and controlling codes used in the communication channel.
- Understand the concepts of convolution codes and analyze the code words using time domain and transform domain approach.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Arrange visits to nearby PSUs such as BHEL, BEL, ISRO, etc., and small-scale communication industries.
3. Show Video/animation films to explain the functioning of various modulation techniques, Channel, and source coding.
4. Encourage collaborative (Group) Learning in the class
5. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize & analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
9. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M–ary PSK, M–ary QAM. Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability. Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation).

Teaching-Learning Process	Chalk and talk method, Simulation of modulation techniques, Power Point Presentation, YouTube videos Animation of BPSK, QPSK, BFSK and DPSK. Problems on Generation and detection of DPSK, QPSK. **Self-study topic**: Minimum shift keying and Non-coherent BFSK **RBT Level:** L1, L2, L3

<table>
<tr><th colspan="2">Module-2</th></tr>
<tr><td colspan="2">Signalling Communication through Band Limited AWGN Channels:
Signalling over AWGN Channels- Introduction, Geometric representation of signals, Gram- Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel (without statistical characterization), Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver.
Signal design for Band limited Channels: Design of band limited signals for zero lSI-The Nyquist Criterion (statement only), Design of band limited signals with controlled lSI-Partial Response signals, Probability of error for detection of Digital PAM: Symbol-by-Symbol detection of data with controlled lSI.</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk & talk method, PowerPoint Presentation, YouTube videos
Self-study topics: Maximum Likelihood detection, Channel equalization
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-3</th></tr>
<tr><td colspan="2">Principles of Spread Spectrum: Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95.</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk & talk method, Seminar about security issues in communication systems
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-4</th></tr>
<tr><td colspan="2">Introduction to Information Theory: Measure of information, Average information content of symbols in long independent sequences.
Source Coding: Encoding of the Source Output, Shannon’s Encoding Algorithm, Shannon-Fano Encoding Algorithm, Huffman coding.
Error Control Coding: Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes.</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, Problems on source coding, error control codes
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-5</th></tr>
<tr><td colspan="2">Linear Block Codes: Matrix description of Linear Block Codes, Error Detection & Correction capabilities of Linear Block Codes, Single error correction Hamming code, Table lookup Decoding using Standard Array.
Convolution codes: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram.</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, Animation of convolution encoders
RBT Level: L1, L2, L3</td></tr>
<tr><td colspan="2">Course outcomes (Course Skill Set)
At the end of the course the student will be able to:
1. Analyze different digital modulation techniques and choose the appropriate modulation technique for the given specifications.
2. Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted bandlimited channels.
3. Differentiate various spread spectrum schemes and compute the performance parameters of communication system.
4. Apply the fundamentals of information theory and perform source coding for given message
5. Apply different encoding and decoding techniques with error Detection and Correction.</td></tr>
<tr><td colspan="2">Assessment Details (both CIE and SEE)</td></tr>
</table>

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8-131-70573-5.
3. K Sam Shanmugam, "Digital and analog communication systems", John Wiley India Pvt. Ltd, 1996.
4. Hari Bhat, Ganesh Rao, "Information Theory and Coding", Cengage, 2017.
5. Todd K Moon, "Error Correction Coding", Wiley Std. Edition, 2006.

Reference Books:

1. Bernard Sklar, "Digital Communications – Fundamentals and Applications", Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
2. K Sam Shanmugam, "Digital and analog communication systems", John Wiley India Pvt. Ltd, 1996.

Web links and Video Lectures (e-Resources)

- https://nptel.ac.in/courses/108102096

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V Semester

Object Oriented Programming with Java & Data Structures			
Course Code	**21EC52**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives:

The goal of the course 'Object Oriented Programming with Java & Data Structures' is

1. To make students learn fundamentals features of object oriented language and JAVA
2. To set up a Java JDK environment to create, debug and run simple Java programs.
3. To Illustrate linear representation of data structures: Stack, Queues, Lists.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop student's theoretical and programming skills.
2. State the need for learning Programming with real-life examples.
3. Support and guide the students for self–study.
4. You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students' progress.
5. Encourage the students for group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lecture activity).
   - As additional examples (post-lecture activity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution of some exercises (post-lecture activity).

Module-1: Introduction to JAVA

An Overview of Java: Object-Oriented Programming, A First Simple program,

Data types, Variables and arrays: Primitive types, Booleans, A Closer Look at Literals, Variables, Type conversion and casting, Arrays,

Introducing Classes: Class fundamentals, Declaring objects, Assigning Object Reference Variables, Introducing Methods, Constructors, The this keyword, Garbage collection, The finalize() method, A stack class.

TextBook 1: Ch: 2, Ch: 3, Ch: 6

Teaching-Learning Process	Chalk and Talk, PowerPoint Presentation **RBT Level:** L1, L2, L3

Module-2: OOP in JAVA

A Closer Look at Methods and classes: Overloading methods, Using objects as parameters, Returning objects, Access control, static members, final members, Command LIne Arguments, String Class.
Inheritance Basics: Member access and Inheritance, A Superclass Variable can reference a subclass object, Using Super, Creating a Multilevel Hierarchy, When Constructors are called.

Text Book 1: Ch: 7

Teaching-Learning	Chalk and Talk, PowerPoint Presentation

Process	**RBT Level:** L1, L2, L3
Module-3: Inheritance and Exception Handling	
Java Collection Framework: Inheritance Hierarchy, Collection interface, The HashSet Class, Generic Collections, Generic methods, Generic Wildcards. Iterators, TreeSet class, LinkedHashset Class, EnumSet Class, List Interface, ArrayList and Vector classes, Linked class, ListIterator interface. Text Book 2: Ch: 4	
Teaching-Learning Process	Chalk and Talk, PowerPoint Presentation **RBT Level:** L1, L2, L3
Module-4: Stack, Queues, Linked data structures	
Stacks: Stack operations, JCF Stack class, A stack interface, An indexed implementation, A linked implementation, Abstracting the common code, Queues: Queue operations, JCF Queue Interface, A simple queue interface, An indexed implementation, Application: A Client-Server system. Text Book 2: Ch: 5, Ch: 6	
Teaching-Learning Process	Chalk and Talk, PowerPoint Presentation **RBT Level:** L1, L2, L3
Module-5: Lists, Trees, Binary Tree	
Lists: JCF list interface, Range-view operation sublist( ), List iterators, Other List types. Tree: Tree definitions, Decision trees, Ordered trees, Traversal algorithms Binary Tree: Definitions, Full binary trees, Complete Binary trees, Binary tree traversal algorithms, Expression tree. Text Book 2: Ch: 7, Ch: 10, Ch: 11	
Teaching-Learning Process	Chalk and Talk, PowerPoint Presentation **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC	
Sl.No	**Experiments**
1	Use Eclipse or NetBeans IDE and acquaint with the various menus. Create a test project, add a test class, and run it. Try debug step by step with a small program of about 10 to 15 lines which contains at least one if else condition and a for loop. To include suitable Small Java programs.
2	Design a class to represent a Student (details include the Student ID, Name of the Student, Branch, year, location and college). Assign initial values using constructor. Design a sub-class with methods to accept the marks & attendance and hence calculate average of marks of 6 subjects and attendance percentage.
3	Write a recursive and non recursive Java program to implement i) Linear search ii) Binary search
4	Write a Java program to implement i) Bubble sort ii) Selection sort iii) quick sort iv) insertion sort
5	Write a Java program to generate 'N' Fibonacci numbers using recursive and non-recursive methods.
6	Write a menu-driven Java program to implement the following data structures using an array: a)Stack ADT (b) Queue ADT
7	Write a menu-driven Java program to implement the following operations on Singly Linked List (SLL): a) Create a SLL of integers. b) Insert a given integer from SLL. c) Delete a given integer into SLL. d) Display the contents of SLL.
8	Write a Java program to perform the following operations:

	a) Insert an element into a Binary Search Tree (BST). b) Delete an element from a BST. c) Search for a key element in a BST d) Traverse the BST in pre-order, in-order & post-order.
9	Write a java program to demonstrate method overloading and constructors overloading.
10	Write a Java programs to implement the following using a singly linked list and perform the given operations. a) Stack ADT i) push an element into stack ii) pop an element from the stack iii) display the contents of the stack
11	Write a Java programs to implement the following using a singly linked list and perform the given operations. b) Queue ADT i) insert an element into queue ii) delete an element from the queue iii) display the contents of the queue
12	Write a java program that works as a simple calculator. Use a Grid Layout to arrange Buttons for digits and for the + - * % operations. Add a text field to display the result. Handle any possible exceptions like divide by zero.

Course Outcomes

At the end of the course the student will be able to:

1. Use OOP concepts effectively to build simple application programs.
2. Set up a Java JDK environment to create, debug and run simple java programs
3. Explain and implement the object oriented core-concepts such as class, object, inheritance and exception handling using JAVA.
4. Implement the data structures such as Arrays, Lists, Stack, Queue and Trees using Java
5. Make a decision on choosing a suitable data structure for a specific application program.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks.

Marks of all experiments' write-ups are added and scaled down to 15 marks.

- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

Suggested Learning Resources:

Text Books

1. "JAVA The Complete Reference", Herbert Schildt, 7th Edition, Tata McGraw Hill, 2007.
2. "Data Structures with Java", John R Hubbard, 2nd edition, Schaum's Outlines.

Reference Books

1. "Fundamentals of OOP and Data Structures in Java", Richard Wiener, Lewis J Pinson, Cambridge University Press, 2000.
2. "Object Oriented Programming and Java", Danny Poo, Derek Kion, Swarnalatha Ashok, Springer, 2nd edition, 2007.
3. "Java Fundamentals", Herbert Schildt, Dale Skrien, McGraw Hill Education, 2017.
4. "Data Structures and Algorithms Made Easy in JAVA: Data Structure and Algorithmic Puzzles", Narasimha Karumanchi, CareerMonk Publications, Second edition, 2011.
5. "Data Structures & Algorithms in Java", Goodrich, Tamassia, Goldwasser, Universities Press; Second edition, 2005.

Web links and Video Lectures (e-Resources):

- VTU e-Shikshana Program
- VTU EDUSAT Program
- https://www.youtube.com/watch?v=CFD9EFcNZTQ
- https://www.youtube.com/watch?v=grEKMHGYyns

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Quizzes, Assignments, Seminars

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V Semester

Computer Communication Networks			
Course Code	**21EC53**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to:

1. Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
2. Understand the protocols associated with each layer.
3. Learn the different networking architectures and their representations.
4. Learn the functions and services associated with each layer.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L): the traditional lecture method, or a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various concepts in networking.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking .
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
6. Demonstrate implementation of various protocols to help better understand the functioning of various concepts in networking.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet. (1.1,1.2, 1.3 (1.3.1to 1.3.4 of Text).

Network Models: TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP. (2.2, 2.3 of Text)

Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP (9.1, 9.2 (9.2.1, 9.2.2))

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of OSI and TCP-IP protocol suites, Example of ARP and RARP. **Self-Study**: Internet standards and administration, **RBT Level:** L1, L2, L3

Module-2

Data Link Control (DLC) services: Framing, Flow and Error Control. (11.1 of Text)

Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. (12.1 of Text).

Connecting Devices: Hubs, Switches, Virtual LANs: Membership, Configuration, Communication between Switches, Advantages. (17.1,17.2 of text)

Wired and Wireless LANs: Ethernet Protocol, Standard Ethernet. (13.1, 13.2 (13.2.1 to 13.2.5 of Text)

Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control. (15.1 of Text)	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animations showing Framing, CSMA, Connecting devices, Problems on ALOHA, CSMA, Framing and Standard ethernet. **Self-Study**: Fast Ethernet, Gigabit ethernet & IEEE802.11 wireless LANs **RBT Level:** L1, L2, L3

Module-3

Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution (18.1(excluding 18.1.3), 18.2, 18.4 of Text)
Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. (19.1of Text), IPv6 addressing and Protocol (22.1 and 22.2).
Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing. (20.1, 20.2 of Text)

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of DHCP, routing protocols, Numericals on Addressing, **Self-Study**: Network Layer performance, RIP, OSPF **RBT Level:** L1, L2, L3

Module-4

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-BackN Protocol, Selective repeat protocol, Piggybacking (23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4, 23.2.5 of Text)

Transport-Layer Protocols in the Internet: User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control L1, L2, L3 Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Error control, TCP congestion control. (24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.6, 24.3.8, 24.3.9 of Text)

***Note: Exclude FSMs for CIE and SEE**

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation/Implementation of Flow control protocols and TCP using simulators, **Self-Study**: Flow Control in TCP **RBT Level:** L1, L2, L3

Module-5

Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client – Server Protocols: Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS. (25.1, 26.1.2, 26.2, 26.3, 26.6 of Text)
Quality of Service (30.1, 30.2.) Network Security (31.1)

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation/Implementation of HTTP, FTP, DNS using network simulators, **Self Study**: WWW , TELNET **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the concepts of networking thoroughly.
2. Identify the protocols and services of different layers.
3. Distinguish the basic network configurations and standards associated with each network.
4. Discuss and analyse the various applications that can be implemented on networks.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end

examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

Reference Books:

1. James J Kurose, Keith W Ross, "Computer Networks", Pearson Education.
2. Wayne Tomasi, "Introduction to Data Communication and Networking", Pearson India, 1st edition.
3. Andrew Tannenbaum, "Computer Networks", Prentice Hall.
4. William Stallings, "Data and Computer Communications", Prentice Hall.

Web links and Video Lectures (e-Resources)

- https://nptel.ac.in/courses/106105183.
- TCP/IP Tutorial and Technical Overview, (IBM Redbook) - Download From http://www.redbooks.ibm.com/abstracts/gg243376.html
- TCP/IP Guide, Charles M Kozierok, Available Online - http://www.tcpipguide.com/
- Request for Comments (RFC) - IETF - http://www.ietf.org/rfc.html
- https://cosmolearning.org/courses/computer-networks-524/video-lectures/
- https://www.eecis.udel.edu/~bohacek/videoLectures/ComputerNetworking/ComputerNetworking_v2.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Implementation of simple networks and various networking protocols and algorithms using simulators like NCTUns / CISCO packet tracer and measurement of various parameters using WireShark
- Implementation of simple networks and various networking protocols and algorithms in C/C++/Python

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V Semester

Microwave Theory and Antennas			
Course Code	**21EC54**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to :

- Describe the microwave properties and its transmission media.
- Describe the microwave devices for several applications.
- Understand the basic concepts of antenna theory.
- Identify antenna types for specific applications.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Using videos for demonstration of the fundamental principles to students for better understanding of concepts.
2. Demonstration of microwave devices and Antennas in the lab environment where students can study them in real time.

Module-1

Microwave Sources: Introduction, Gunn Diode (Text 2: 7.1,7.1.1,7.1.2)

Microwave transmission lines: Microwave frequencies, Microwave devices, Microwave systems. Transmission line equations and solutions, Reflection Coefficient and Transmission Coefficient. Standing wave and standing wave ratio. Smith chart, Single stub matching.

Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 (except double stub matching)

Teaching-Learning Process	Chalk and Talk would be helpful for the quantitative analysis. Videos of the Basic principles of the devices would help students to grasp better. **RBT Level:** L1, L2, L3

Module-2

Microwave Network Theory: Introduction, S matrix representation of multi-port networks (Text 1: 6.1, 6.3, 6.3.1, 6.3.2)

Microwave passive devices: Coaxial connectors and Adapters, Attenuators, Phase shifters, waveguide Tees, Magic Tee, Circulator, Isolator. (Text 1: 6.4.2, 6.4.14, 6.4.15, 6.4.16, 6.4.17 A, B)

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3

Strip Lines: Introduction, Microstrip lines, Parallel Strip lines (Text 2: 11.1,11.2)

Antenna Basics: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam efficiency, Directivity and Gain, Antenna Aperture Effective height, Bandwidth, Radio communication Link, Antenna Field Zones (Text 3: 2.1-2.7, 2.9-2.11, 2.13).

Teaching-Learning Process	Chalk and talk method, Power point presentation and videos. **RBT Level:** L1, L2, L3

Module-4	
Point sources and arrays: Introduction, Point Sources, Power patterns, Power theorem, Radiation Intensity, Arrays of 2 isotropic point sources, Pattern multiplication, Linear arrays of n Isotropic sources of equal amplitude and Spacing. (Text 3: 5.1-5.6, 5.9, 5.13) **Electric Dipole**: Introduction, Short Electric dipole, Fields of a short dipole. Radiation resistance of a short dipole. Thin linear antenna (field analysis). (Text 3: 6.1-6.5)	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Loop and Horn antenna: Introduction: Small loop, Comparison of far fields of small loop and Short dipole. Radiation resistance of small loop, Horn Antennas, Rectangular antennas. (Text 3: 7.1,7.2, 7.4, 7.6, 7.7, 7.8, 7.19, 7.20) **Antenna Types**: The Helix geometry, Helix modes, Practical design consideration for mono-filar axial mode Helical Antenna, Yagi Uda array, Parabolic Reflector (Text 3: 8.3, 8.4, 8.5, 8.8, 9.5)	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Describe the use and advantages of microwave transmission
2. Analyze various parameters related to transmission lines.
3. Identify microwave devices for several applications.
4. Analyze various antenna parameters and their significance in building the RF system.
5. Identify various antenna configurations for suitable applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per

the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1. Microwave Engineering -Annapurna Das, Sisir K Das, TMH Publication, 2nd Edition, 2010.
2. Microwave Devices and Circuits – Samuel Y Liao, Pearson Education.
3. Antennas and Wave Propagation -John D Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition, McGraw Hill Education, 2013.

Reference Books:

1. Microwave Engineering -David M Pozar, John Wiley India Pvt Ltd., Pvt Ltd., 3rd edition, 2008.
2. Microwave Engineering-Sushrut Das, Oxford Higher Education, 2nd Edn, 2015.
3. Antennas and Wave Propagation- Harish and Sachidananda, Oxford University Press, 2007.

Web links and Video Lectures (e-Resources)

- Nptel Videos and Lectures
- https://www.tutorialspoint.com/antenna_theory/antenna_theory_horn.html
- http://www.antenna-theory.com/antennas/smallLoop.php

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Lab based demos for the devices can be done in the form of experiments.
- Mini Projects can be given to students involving design of microwave devices and Antennas.

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V Semester

Communication Lab II			
Course Code	**21ECL55**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Design and demonstrate communication circuits for different digital modulation techniques.
- To simulate Source coding Algorithms using C/C++/ MATLAB code.
- To simulate Error correcting and detecting codes using C/C++/ MATLAB code.
- Simulate the networking concepts and protocols using C/C++/ Network simulation tool.
- Understand entropies and mutual information of different communication channels.

Sl.No.	**Experiments**
	Implement the following using discrete components
1	FSK generation and detection
2	PSK generation and detection
3	DPSK Transmitter and receiver
4	QPSK Transmitter and Receiver
	Implement the following in C/C++/MATLAB/Scilab/Python or any other Suitable software
5	Write a program to encode binary data using Huffman code and decode it.
6	Write a program to encode binary data using a (7,4) Hamming code and decode it.
7	Write a program to encode binary data using a ((3,1,2)/suitably designed) Convolution code and decode it.
8	For a given data, use CRC-CCITT polynomial to obtain the CRC code. Verify the program for the cases a) Without error b) With error
	Implement the following algorithms in C/C++/MATLAB/Network simulator
9	Write a program for congestion control using leaky bucket algorithm.
10	Write a program for distance vector algorithm to find suitable path for transmission.
11	Write a program for flow control using sliding window protocols.
12	Configure a simple network (Bus/star) topology using simulation software **OR** Configure a simple network (Ring/Mesh) topology using simulation software.
	Demonstration Experiments (For CIE)
13	Configure and simulate simple Wireless Local Area network.
14	Simulate the BER performance of (2, 1, 3) binary convolutional code with generator sequences g(1) =(1 0 1 1) and g(2) =(1 1 1 1) on AWGN channel. Use QPSK modulation scheme. Channel decoding is to be performed through Viterbi decoding. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus E_b/N_0. Consider binary input vector of size 3 lakh bits. Also find the coding gain.
15	Simulate the BER performance of (7, 4) Hamming code on AWGN channel. Use QPSK modulation

	scheme. Channel decoding is to be performed through maximum-likelihood decoding. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus E_b/N_0. Consider binary input vector of size 5 lakh bits. Use the following parity check matrix for the (7, 4) Hamming code. Also find the coding gain. $$H = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 \end{bmatrix}$$
16	Simulate the BER performance of rate 1/3 Turbo code. Turbo encoder uses two recursive systematic encoders with $G(D) = \left[1, \frac{1+D^4}{1+D+D^2+D^3+D^4}\right]$ and pseudo-random interleaver. Use QPSK modulation scheme. Channel decoding is to be performed through maximum a-posteriori (MAP) decoding algorithm. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus E_b/N_0. Consider binary input vector of size of around 3 lakh bits and the block length as 10384 bits. Also find the coding gain.

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

1. Design and test the digital modulation circuits and display the waveforms.
2. To Implement the source coding algorithm using C/C++/ MATLAB code.
3. To Implement the Error Control coding algorithms using C/C++/ MATLAB code.
4. Illustrate the operations of networking concepts and protocols using C programming and network simulators.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by

the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. K Sam Shanmugam, "Digital and analog communication systems", John Wiley India Pvt. Ltd, 1996.
3. Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

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V Semester

IoT (Internet of Things) Lab			
Course Code	21EC581	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- To impart necessary and practical knowledge of components of Internet of Things
- To develop skills required to build real-life IoT based projects.

Sl.No	**Experiments**
1	i) To interface LED/Buzzer with Arduino/Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds. ii) To interface Push button/Digital sensor (IR/LDR) with Arduino/Raspberry Pi and write a program to 'turn ON' LED when push button is pressed or at sensor detection.
2	i) To interface DHT11 sensor with Arduino/Raspberry Pi and write a program to print temperature and humidity readings. ii) To interface OLED with Arduino/Raspberry Pi and write a program to print temperature and humidity readings on it.
3	To interface motor using relay with Arduino/Raspberry Pi and write a program to 'turn ON' motor when push button is pressed.
4	To interface Bluetooth with Arduino/Raspberry Pi and write a program to send sensor data to smartphone using Bluetooth.
5	To interface Bluetooth with Arduino/Raspberry Pi and write a program to turn LED ON/OFF when '1'/'0' is received from smartphone using Bluetooth.
6	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to thingspeak cloud.
7	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from thingspeak cloud.
8	To install MySQL database on Raspberry Pi and perform basic SQL queries.
9	Write a program on Arduino/Raspberry Pi to publish temperature data to MQTT broker.
10	Write a program to create UDP server on Arduino/Raspberry Pi and respond with humidity data to UDP client when requested.
11	Write a program to create TCP server on Arduino/Raspberry Pi and respond with humidity data to TCP client when requested.
12	Write a program on Arduino/Raspberry Pi to subscribe to MQTT broker for temperature data and print it.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Understand internet of Things and its hardware and software components
2. Interface I/O devices, sensors & communication modules
3. Remotely monitor data and control devices
4. Develop real life IoT based projects

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Vijay Madisetti, Arshdeep Bahga, Internet of Things. "A Hands on Approach", University Press
2. Dr. SRN Reddy, Rachit Thukral and Manasi Mishra, "Introduction to Internet of Things: A practical Approach", ETI Labs
3. Pethuru Raj and Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
4. Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
5. Adrian McEwen, "Designing the Internet of Things", Wiley
6. Raj Kamal, "Internet of Things: Architecture and Design", McGraw Hill

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V Semester

Communication Simulink Toolbox			
Course Code	**21EC582**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- To impart knowledge of simulation software in digital communications
- To develop skills required to build and analyze the performance of various simulated communication systems under different conditions

Sl. No.	Experiments
1	Modulation & demodulation of a random binary data stream using 16 – QAM.
2	Bit error rate (BER) improvement using Pulse Shaping on 16 – QAM signal. (Use forward error correction (FEC) coding.)
3	Perform OFDM modulation and obtain time domain and frequency domain plots to show a low-rate signal, a high-rate signal, and a frequency selective multipath channel response.
4	(a) Simulate basic OFDM with no cyclic prefix. (b) Perform Equalization, Convolution, and Cyclic Prefix Addition on basic OFDM.
5	OFDM with FFT Based Oversampling - Modify an OFDM+ Cyclic Prefix signal to efficiently output an oversampled waveform from the OFDM modulator.
6	Simulate a basic communication system in which the signal is first QPSK modulated and then subjected to Orthogonal Frequency Division Multiplexing (OFDM).
7	Obtain the scatter plots & eye diagrams of a QPSK signal to visualize the signal behaviour in presence of AWGN.
8	(a) Generate a multiband signal using the Communications Toolbox. (b) Random noise generation using Simulink & display histogram plots of Gaussian, Rayleigh, Rician, and Uniform noise.
9	QPSK Transmitter and Receiver in Simulink.
10	Multipath Fading Channel in Simulink – For example: Simulate QPSK transmission over a • multipath Rayleigh fading channel and • a multipath Rician fading channel.
11	Adjacent and Co-Channel Interference using Simulink. • Use PSK-modulated signals to show the effects of adjacent and co-channel interference on a transmitted signal.
12	Modulation Classification with Deep Learning • Predict Modulation Type Using CNN

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Perform sampling, aliasing, filtering, and quadrature modulation through simulation.
2. Plot signal space representation of digital modulation techniques.
3. Design and implement a pulse shape and matched filter to avoid inter-symbol interference and maximize receiver SNR.
4. Demonstrate advanced wireless communication techniques like Multipath fading, CCI etc. and model the same using MATLAB / Simulink.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Communication Toolbox – Examples (https://in.mathworks.com/)
2. "Digital Communication Laboratory" Courseware by Professor Lee C Potter, Dr. Yang Yang, Electrical and Computer Engineering, The Ohio State University.

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V Semester

Antenna Design & Testing			
Course Code	**21EC583**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0: 2 :0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- To understand the various antenna parameters.
- Conduct experiments to study the Radiation pattern of Antennas.
- Design different types of antenna arrays and study the pattern characteristics (MATLAB)
- Design of MMIC antennas like Patch Antenna and study the characteristics.

Sl.No	**Experiments**
1	To obtain the radiation pattern of a Yagi-Uda Antenna array and calculate its directivity.
2	To obtain the radiation pattern of a Dipole Antenna array and calculate its directivity.
3	To calculate the aperture of a Dipole Antenna.
4	To obtain the near and far fields of a given antenna and compare the fields.
5	To obtain the Radiation pattern of a microstrip antenna.
6	To obtain the resonant frequency of a Yagi-Uda /Dipole antenna.
7	To obtain the bandwidth of a given Antenna.
8	Plot 2-D and 3-D radiation pattern of omnidirectional antenna using MATLAB.
9	Design and implementation of a broadside array using MATLAB.
10	Design and implementation of an endfire array using MATLAB.
Demonstration Experiments (For CIE)	
11	Design of a Patch Antenna using HFSS Software.
12	Design of a dipole Antenna using HFSS Software.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Analyze the radiation pattern and characteristics of antenna
2. Ability to design various antenna
3. Ability to use different software tools to study antenna characteristics
4. Analyze radiation pattern of linear array antennas

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning

of the practical session.

- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Antennas and Wave Propagation -John D Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition, McGraw Hill Education, 2013.
2. https://www.mathworks.com/help/antenna/
3. Help and demo files of the HFSS and MATLAB software

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V Semester

Microwaves Toolbox			
Course Code	**21EC584**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	03

Course objectives:

- Identification of microwave components/devices.
- Study basic principles of operation of microwave devices/ components

Sl.No	**Experiments**
1	V- I Characteristics of Gunn-diode.
2	Study of characteristics of Magic Tee.
3	Coupling and Isolation characteristics of microstrip directional coupler.
4	Determination of power division of microstrip power divider.
5	Determination of resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
6	Measurement of frequency, guide wavelength, power and attenuation in a microwave Test bench.
7	Study of characteristics of E plane Tee / H plane Tee.
8	To measure unknown impedance using Smith chart through test bench setup.
9	Measurement of VSWR and reflection coefficient and attenuation in a microwave test bench setup.
10	Study propagation of wave using rectangular waveguide using MATLAB.
11	Study of impedance matching using MATLAB.
12	To calculate phase and group velocity using MATLAB.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the characteristics of microwave sources.
2. Demonstrate the characteristics of directional coupler
3. Study of microwave measurement procedure.
4. Apply MATLAB toolbox for study of microwaves phenomena.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.

- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

MATLAB

1. Microwave Engineering -Annapurna Das, Sisir K Das, TMH Publication, 2nd Edition, 2010.
2. Antennas and Wave Propagation -John D Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition, McGraw Hill Education, 2013.
3. https://www.mathworks.com/help/antenna
4. https://www.mathworks.com/help/antenna/ref/waveguide.html

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VI Semester

Computer Organization & ARM Microcontrollers			
Course Code	**21EC62**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

1. Explain the basic organization of a computer system.
2. Demonstrate functioning of different sub systems, such as processor, Input/output, and memory.
3. Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.
4. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
5. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Give Programming Assignments.

Module-1

Basic Structure of Computers: Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement.
Text Book 1: Chapter 1 – 1.3, 1.4, 1.6 (1.6.1-1.6.4, 1.6.7), Chapter 2 – 2.2 to 2.10
Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Direct Memory Access, Buses, Interface Circuits, Standard I/O Interfaces – PCI Bus, SCSI Bus, USB.
Text Book 1: Chapter 4 – 4.1, 4.2, 4.4, 4.5, 4.6, 4.7

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-2

Memory System: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, Performance Considerations.
Text book 1: Chapter 5 – 5.1 to 5.4, 5.5 (5.5.1, 5.5.2), 5.6

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hard-wired Control, Micro programmed Control. Basic concepts of pipelining,

Text book 1: Chapter7, Chapter 8 – 8.1

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-3

ARM Embedded Systems: Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications.
ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions.
Text book 2: Chapter 1, 2

Teaching-Learning Process	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-4

Introduction to the ARM Instruction set: Introduction, Data processing instructions, Load - Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution.
Text book 2: Chapter 3

Teaching-Learning Process	Chalk and Talk, Power point presentations, Programming assignments **RBT Level:** L1, L2, L3

Module-5

Introduction to the THUMB instruction set: Introduction, THUMB register usage, ARM – THUMB interworking, Other branch instructions, Data processing instructions, Stack instructions, Software interrupt instructions.
Efficient C Programming: Overview of C Compilers and optimization, Basic C Data types, C looping structures.
Text book 2: Chapter 4, 5

Teaching-Learning Process	Chalk and Talk, Power point presentations, Programming assignments **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Conduct the following experiments by writing Assembly Language Program (ALP) using ARM Cortex M3 Registers using an evaluation board/simulator and the required software tool.

Sl.No	Experiments
1	Write an ALP to i) multiply two 16-bit binary numbers. ii) add two 64-bit numbers.
2	Write an ALP to find the sum of first 10 integer numbers.
3	Write an ALP to find factorial of a number.
4	Write an ALP to add an array of 16-bit numbers and store the 32-bit result in internal RAM.
5	Write an ALP to find the square of a number (1 to 10) using look-up table.
6	Write an ALP to find the largest/smallest number in an array of 32 numbers.
7	Write an ALP to arrange a series of 32-bit numbers in ascending/descending order.
8	i) Write an ALP to count the number of ones and zeros in two consecutive memory locations. ii)Write an ALP to Scan a series of 32-bit numbers to find how many are negative.

Demonstration Experiments (For CIE only not for SEE)	
Conduct the following experiments on an ARM CORTEX M3 evaluation board using evaluation version of Embedded 'C' & Keil µvision-4 tool/compiler.	
9	Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
10	Interface a DAC and generate Triangular and Square waveforms.
11	Display the Hex digits 0 to F on a 7-segment LED interface, with a suitable delay in between.
12	Interface a simple Switch and display its status through Relay, Buzzer and LED.

Course Outcomes

At the end of the course the student will be able to:

1. Explain the basic organization of a computer system.
2. Demonstrate functioning of different sub systems, such as processor, Input/output, and memory.
3. Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.
4. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

Suggested Learning Resources:

Textbooks

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th Edition, Tata McGraw Hill, 2002. (Listed topics only from Chapters 1, 2, 4, 5, 8).
2. Andrew N Sloss, Dominic System and Chris Wright, “ARM System Developers Guide”, Elsevier, Morgan Kaufman publisher, 1st Edition, 2008.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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VI Semester

VLSI Design and Testing			
Course Code	**21EC63**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Impart knowledge of MOS transistor theory and CMOS technology
- Learn the operation principles and analysis of inverter circuits.
- Infer the operation of Semiconductor memory circuits.
- Demonstrate the concept of CMOS testing.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Arrange visits to nearby PSUs and industries.
3. Show Video/animation films to explain the functioning of various fabrication & testing techniques.
4. Encourage collaborative (Group) Learning in the class
5. Topics will be introduced in multiple representations.
6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: A Brief History, MOS Transistors, CMOS Logic (1.1 to 1.4 of TEXT1)

MOS Transistor Theory: Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (2.1, 2.2, 2.4 and 2.5 of TEXT1).

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on transistor working **Self-study topics**: MOSFET Scaling and Small-Geometry Effects **RBT Level:** L1, L2, L3

Module-2

Fabrication: CMOS Fabrication and Layout, Introduction, CMOS Technologies, Layout Design Rules, (1.5 and 3.1 to 3.3 of TEXT1).

Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths (4.1 to 4.5 of TEXT1, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).

Teaching-Learning Process	Chalk and talk method, Power point presentation, YouTube videos, Videos on fabrication **Self-study topics**: Layouts of complex design using Euler's method **RBT Level:** L1, L2, L3

Module-3

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM) (10.1 to 10.6 of TEXT2)

Teaching-Learning	Chalk and talk method, PowerPoint Presentation, YouTube videos on Standard

Process	cell memory Design **Self-study topics**: Memory array design **RBT Level:** L1, L2, L3
Module-4	
Faults in digital circuits: Failures and faults, Modelling of faults, Temporary faults **Test generation for combinational logic circuits**: Fault diagnosis of digital circuits, test generation techniques for combinational circuits, Detection of multiple faults in combinational logic circuits. (1.1 to 1.3, 2.1 to 2.3 of TEXT3)	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, videos on testing algorithms for test generation **Self-study topics**: Testable combinational logic circuits **RBT Level:** L1, L2, L3
Module-5	
Test generation for sequential circuits: Testing of sequential circuits as iterative combinational circuits, state table verification, test generation based on circuits structure, functional fault models, test generation based on functional fault models. **Design of testable sequential circuits**: Controllability and Observability, Adhoc design rules, design of diagnosable sequential circuits, The scan path technique, LSSD, Random Access scan technique, partial scan. (4.1 to 4.5, 5.1 to 5.7 of TEXT3)	
Teaching-Learning Process	Chalk and talk method/Power point presentation, YouTube videos **Self-study topics**: Memory testing techniques **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
2. Draw the basic gates using the stick and layout diagram with the knowledge of physical design aspects.
3. Interpret memory elements along with timing considerations.
4. Interpret testing and testability issues in combinational logic design.
5. Interpret testing and testability issues in combinational logic design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20**

Marks (duration 01 hours)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.
3. "Digital Circuit Testing and Testability", Lala Parag K, New York, Academic Press, 1997.

Reference Books:

1. "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.
2. "Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits", Vishwani D Agarwal, Springer, 2002.

Web links and Video Lectures (e-Resources)

- https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM
- https://www.youtube.com/watch?v=lRpt1fCHd8Y&list=PLCmoXVuSEVHlEJi3SwdyJ4EICffuyqpjk
- https://www.youtube.com/watch?v=yLqLD8Y4-Qc

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Model displayed for clear understanding of fabrication process of MOS transistor
- Practise session can be held to understand the significance of various layers in MOS process, with the help of coloured layouts

03.10.2022

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VI Semester

VLSI Laboratory			
Course Code	**21ECL66**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Design, model, simulate and verify digital circuits.
- Design layouts and perform physical verification of CMOS digital circuits.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist.
- Perform RTL-GDSII flow and understand the stages in ASIC.

Sl.No.	**Experiments**
	ASIC Digital Design
1	4-Bit Adder • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
2	4-Bit Booth Multiplier • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
3	32-Bit ALU Supporting 4-Logical and 4-Arithmetic operations, using case and if statement for ALU Behavioral Modeling • Write Verilog Code • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist • Identify Critical path
4	Latch and Flip-Flop • Synthesize the design and compare the synthesis report (D, SR, JK)
	ASIC Analog Design
5	a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of Inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:

	i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and the time period of 20ns and plot the input voltage and output voltage of designed inverter? ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width? iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter? b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.
6	a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results. b) Draw the layout of NAND with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.
7	a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measure the Unit Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB. b) Draw Layout of common source amplifier, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.
8	a) Capture schematics of two-stage operational amplifier and measure the following: i. UGB ii. dB Bandwidth iii. Gain Margin and phase margin with and without coupling capacitance iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality. v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in part a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.
	Demonstration Experiments (For CIE)
9	UART • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist, Identify Critical path
10	For synthesized netlist carry out the following: • Floor planning • Placement and Routing • Record the parameters such as no. of metal layers used for routing, flip method for placement of standard cells • Physical Verification and record the DRC and LVS reports • Generate GDSII

11	Design and characterize 6T binary SRAM cell and measure the following: • Read Time, Write Time, SNM, Power • Draw Layout of 6T SRAM, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

1. Design and simulate combinational and sequential digital circuits using Verilog HDL.
2. Understand the synthesis process of digital circuits using EDA tool.
3. Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist.
4. Design and simulate basic CMOS circuits like inverter, common source amplifier, differential amplifier, SRAM.
5. Perform RTL_GDSII flow and understand the stages in ASIC design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.
(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be

decided jointly by examiners.
Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours.
Rubrics suggested in Annexure-II of Regulation book

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VI Semester

Communication Engineering			
Course Code	**21EC651**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0: 1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

This course will enable students to:

- Describe essential elements of an electronic communication system.
- Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
- Define the sampling theorem and methods to generate pulse modulations.
- Learn the various methods of digital modulation techniques and compare the different schemes.
- Introduce the basic concepts of information theory and coding.
- Understand the basic concepts of wireless and cellular communications.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, Signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation (Text 1: 1.1 to 1.10)

Teaching-Learning Process	Chalk and talk method, Power Point Presentation **Self-study topics:** Classification of Signals and systems **RBT Level:** L1, L2, L3

Module-2

Amplitude Modulation Techniques: Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, (TEXT 1: 4.1, 4.2, 4.4, 4.6)

Angle Modulation Techniques: Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation (TEXT1: 5.1, 5.2, 5.5)

Teaching-Learning Process	Chalk and talk method/Power point presentation **Self-study topics:** DSBSC, SSB and VSB modulation techniques and comparison. **RBT Level:** L1, L2, L3

Module-3	
Sampling Theorem and Pulse Modulation Techniques: Digital Versus Analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals (TEXT 1: 7.2 to 7.8)	
Teaching-Learning Process	Chalk and talk method **Self-study topics:** Differential PCM and Delta Modulation **RBT Level:** L1, L2, L3
Module-4	
Digital Modulation Techniques: Types of digital Modulation, ASK, FSK, PSK, QPSK. (TEXT 1: 9.1 to 9.5) **Information Theory, Source and Channel Coding:** Information, Entropy and its properties, Shannon,-Hartley Theorem, Objectives of source coding, Source coding technique, Shannon source coding theorem, Channel coding theorem, Error Control and Coding. [Text1: 10.1,10.2, 10.11.2, 11.1 to 11.3, 11.8, 11.9, 11.12]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Quadrature Amplitude Modulation, Comparison of Digital Modulation techniques. **RBT Level:** L1, L2, L3
Module-5	
Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next generation networks, Applications of wireless communication (TEXT 2: 1.1 to 1.7) **Principles of Cellular Communications:** Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequency reuse distance (TEXT 2: 4.1 to 4.7)	
Teaching-Learning Process	Chalk and talk method/Power point presentation **Self-study topics:** Basic propagation mechanisms, Multipath fading. **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Describe the scheme and concepts of radiation and propagation of communication signals through air.
2. Understand the AM and FM modulation techniques and represent the signal in time and frequency domain relations.
3. Understand the process of sampling and quantization of signals and describe different methods to generate digital signals.
4. Describe the basic digital modulation techniques, channel capacity, source coding technique and the channel coding.
5. Compare the different wireless communication systems and describe the structure of cellular communication.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Books:

1. T L Singal, Analog and Digital Communications, McGraw Hill Education (India) Private Limited, 2012, 0-07-107269-1
2. T L Singal, Wireless Communications, McGraw Hill Education (India) Private Limited, 2016, ISBN:0-07-068178-3.

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VI Semester

Microcontrollers			
Course Code	**21EC652**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

This course will enable students to:

- Understand the difference between a Microprocessor and a Microcontroller and embedded microcontrollers.
- Familiarize the basic architecture of 8051 microcontroller.
- Program 8051microprocessor using Assembly Level Language and C.
- Understand the interrupt system of 8051 and the use of interrupts.
- Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051.
- Interface 8051 to external memory and I/O devices using its I/O ports.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
8. Give Programming Assignments.

Module-1

8051 Microcontroller: Microprocessor Vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing.
Text2 : Chapter 1 section 1.1 to 1.3, chapter 3 sections 3.1 to 3.3

Teaching-Learning Process	Chalk and talk method, Simulation of modulation techniques **RBT Level:** L1, L2, L3

Module-2

8051 Instruction Set: Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions.
Text2 : Chapter 5 , chapter 6, chapter 7, chapter 8

Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3

Module-3	
8051 Jump and Call instructions & Embedded C Jump and Call Instructions, Calls & Subroutine instructions. Assembly language program examples on subroutine and involving loops. Text2 : chapter 8 section 8.1 to 8.4 **8051 Programming in C**: Data Types and Time delay in 8051 C, I/O programming in 8051 C, Logical Operations in C. Text1 : chapter 7 section 7.1 to 7.3	
Teaching-Learning Process	Chalk and talk method **RBT Level:** L1, L2, L3
Module-4	
8051 Timers and Serial Port **8051 Timers and Counters** – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode- 2 on a port pin. **8051 Serial Communication**- Basics of Serial Data Communication, RS- 232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially. Text1 : Chapter 9 section 9.1 Chapter 10 section 10.1 to 10.5	
Teaching-Learning Process	Chalk and talk method **RBT Level:** L1, L2, L3
Module-5	
8051 Interrupts and Interfacing Applications 8051 Interrupts. 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a Timer interrupt. **Interfacing** 8051 to ADC-0804, DAC, LCD and Stepper motor and their 8051 Assembly and C language interfacing programming. Text 1: Chapter 11 section 11.1 and 11.2 Chapter 13 section 13.1 to 13.2, chapter 12 section 12.1, chapter 17 section 17.2	
Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Explain the difference between Microprocessors & Microcontrollers, Architecture of 8051 Microcontroller, Interfacing of 8051 to external memory and Instruction set of 8051.
2. Develop 8051 Assembly level programs using 8051 instruction set.
3. Develop 8051 Assembly / C language program to generate timings and waveforms using 8051 timers, to send & receive serial data using 8051 serial port.
4. Develop 8051 Assembly / C language programs to generate square wave on 8051 I/O port pin using interrupt and C Programme to send & receive serial data using 8051 serial port.
5. Interface various peripheral devices to 8051 using I/O ports.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester

3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. "The 8051 Microcontroller and Embedded Systems – using assembly and C", Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D McKinlay; PHI, 2006 / Pearson, 2006.
2. "The 8051 Microcontroller", Kenneth J Ayala, 3rd Edition, Thomson/Cengage Learning.

Reference Books:

1. "The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.
2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

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(Effective from the academic year 2021 – 22)

VI Semester

Basic VLSI Design			
Course Code	**21EC653**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Impart knowledge on architectural choices and performance trade-offs involved in designing and realizing the circuits in CMOS technology
- Cultivate the concepts of subsystem design processes
- Demonstrate the concepts of CMOS testing

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
8. Incorporate programming examples given under Activity based learning.

Module-1

Introduction: A Brief History, MOS Transistors, MOS Transistor Theory, Ideal I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (1.1, 1.3, 2.1, 2.2, 2.4, 2.5 of TEXT2).
Fabrication: nMOS Fabrication, CMOS Fabrication [P-well process, N-well process, Twin tub process], BiCMOS Technology (1.7, 1.8, 1.10 of TEXT1).

Teaching-Learning Process	Chalk and talk method, YouTube videos, Power point presentation **RBT Level:** L1, L2

Module-2

MOS and BiCMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout.
Basic Circuit Concepts: Sheet Resistance, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads (3.1 to 3.3, 4.1, 4.3 to 4.8 of TEXT1).

Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Scaling of MOS Circuits: Scaling Models & Scaling Factors for Device Parameters **Subsystem Design Processes**: Some General considerations, An illustration of Design Processes, **Illustration of the Design Processes**: Regularity, Design of an ALU Subsystem, The Manchester Carry-chain and Adder Enhancement Techniques (5.1, 5.2, 7.1, 7.2, 8.2, 8.3, 8.4.1, 8.4.2 of TEXT1).	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Subsystem Design: Some Architectural Issues, Switch Logic, Gate (restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA) (6.1 to 6.3, 6.4.1, 6.4.3, 6.4.6 of TEXT1). **FPGA Based Systems**: Introduction, Basic concepts, Digital design and FPGAs, FPGA based System design, FPGA architecture, Physical design for FPGAs (1.1 to 1.4, 3.2, 4.8 of TEXT3).	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Memory, Registers and Aspects of system Timing: System Timing Considerations, Some commonly used Storage/Memory elements (9.1, 9.2 of TEXT1). **Testing and Verification**: Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability (12.1, 12.1.1, 12.3, 12.5, 12.6 of TEXT 2).	
Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
3. Interpret Memory elements along with timing considerations
4. Demonstrate knowledge of FPGA based system design
5. Interpret testing and testability issues in VLSI Design
6. Analyze CMOS subsystems and architectural issues with the design constraints.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. "Basic VLSI Design"- Douglas A Pucknell & Kamran Eshraghian, PHI, 3rd Edition.
2. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
3. "FPGA Based System Design", Wayne Wolf, Pearson Education, 2004, Technology and Engineering.

Web links and Video Lectures (e-Resources)

- https://nptel.ac.in/courses/117101058
- https://nptel.ac.in/courses/117106093
- https://youtu.be/9SnR3M3CIm4
- https://nptel.ac.in/courses/108/107/108107129/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Wherever necessary **Cadence/Synopsis/Menta Graphics tools** must be used.

1.Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

i. An inverter
ii. A Buffer
iii. Transmission Gate
iv. Basic/universal gates
v. Flip flop -RS, D, JK, MS, T
vi. Serial & Parallel adder
vii. 4-bit counter [Synchronous and Asynchronous counter]

2. Design an op-amp with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:

a. Draw the schematic and verify the following
i) DC Analysis
ii) AC Analysis
iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design.

03.10.2022

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VI Semester

Electronic Circuits with Verilog			
Course Code	**21EC654**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- To understand the basic Verilog HDL design flow.
- To understand the basic Verilog programming concepts.
- To describe the simple logic circuits using dataflow, gate-level, and behavioural level modelling.
- To model digital systems using advanced concepts of Verilog HDL.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
8. Give programming assignments.

Module-1

Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs. (Text 1)
Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. (Text 1)

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

Basic Concepts: Lexical conventions, datatypes, system tasks, compiler directives. (Text 1)
Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing. (Text 1)

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3

Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. (Text1)
Dataflow Modeling: Continuous assignments, delay specification, expressions, operators, operands, operator types. (Text 1)

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-4

Behavioral Description: Behavioral Description Highlights, Structure of the HDL Behavioral Description, Sequential Statements, IF Statement, The case Statement , Verilog casex and casez The wait-for Statement. The Loop Statement, For-Loop, While-Loop, Verilog repeat, Verilog forever (content with respect to Verilog only) (Text 2)

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-5

Structural Description: Highlights of Structural Description, Organization of Structural Description Binding (4.1, 4.2, 4.3 till example 4.9) (Text 2)
Tasks and Functions: Differences between tasks and functions, declaration, invocation, automatic tasks and functions. (Text 1)

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)
At the end of the course the student will be able to:

1. Under the Verilog HDL design flow.
2. Describe the basic concepts of Verilog HDL programming.
3. Design of digital electronics circuits using dataflow, behavioural, gate-level, and structural modelling.
4. Design complex digital circuits using advanced Verilog concepts.

Assessment Details (both CIE and SEE)
The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:
Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**
(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).
CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.
Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. "Verilog HDL: A Guide to Digital Design and Synthesis", Samir Palnitkar, Pearson education, Second edition.
2. "HDL programming (VHDL and Verilog)", Nazeih M Botros, John Wiley India Pvt. Ltd., 2008.

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VI Semester

Sensors & Actuators			
Course Code	**21EC655**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- To provide the fundamental knowledge about sensors and measurement system.
- To impart the knowledge of static and dynamic characteristics of instruments and understand the factors in selection of instruments for measurement.
- To discuss the principle, design and working of transducers for the measurement of physical time varying quantities.
- Understand the working of various actuators suitable in industrial process control systems.
- Understand the principle and application of smart sensors.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Explain the fundamental concepts required for the module in the introduction phase for the module.
2. Conducting quiz after completion of every module in class and evaluate.
3. Asking questions about completed previous topic, will aid to assess the student understanding.
4. Evaluate the internals answer booklet by correcting the mistakes if any.
5. Modules revision at the end as well use practical lab sessions and demonstrate the concepts if applicable and feasible.

Module-1

Sensors and measurement system: Sensors and transducers, Classifications of transducers-primary & secondary, active & passive, analog and digital transducers. Smart sensors.

Measurement: Definition, significance of measurement, instruments and measurement systems. mechanical, electrical and electronic instruments. Elements of generalized measurement system with example. Input-output configuration of measuring instruments and measurement systems, methods of correction for interfering and modifying inputs.

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, More examples relating to applications **RBT Level:** L1, L2, L3

Module-2

Static and Dynamic Characteristics: Static calibration and error calibration curve, accuracy and precision, indications of precision, static error, scale range and scale span, reproducibility and drift, repeatability, signal to noise ratio, sensitivity, linearity, hysteresis, threshold, dead zone and dead time, resolution, signal to noise ratio, factors influencing the choice of transducers/instruments.

Dynamic response – Dynamic characteristics, Transfer function of generalized first order system, time constant. Transfer function of generalized second order system, natural frequency and Damping ratio.

Teaching-Learning Process	Chalk and talk method, Power point presentation, VI Lab to demonstrate the characteristics of sensors, More examples relating to applications **RBT Level:** L1, L2, L3

Module-3	
Measurement of Temperature: RTD, Thermistor, Thermocouple, laws of thermocouple, Thermopile, AD590. **Measurement of Displacement**: Introduction, Principles of Transduction, Variable resistance devices, variable Inductance Transducer, Variable Capacitance Transducer, Hall Effect Devices, Proximity Devices, Digital Transducer.	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, Virtual instrumentation Lab to demonstrate the characteristics of sensors **RBT Level:** L1, L2, L3
Module-4	
Measurement of Strain: Introduction, Types of Strain Gauges, Theory of operation of resistance strain gauges, Types of Electrical Strain Gauges –Wire gauges, unbounded strain gauges, foil gauges, semiconductor strain gauges (principle, types & list of characteristics only), Strain gauge Circuits – Wheatstone bride circuit, Applications. **Measurement of Force & Torque:** Introduction, Force measuring sensor –Load cells – column types devices, proving rings, cantilever beam, pressductor. Hydraulic load cell, electronic weighing system. Torque measurement: Absorption type, transmission type, stress type & deflection type.	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, More examples relating to applications **RBT Level:** L1, L2, L3
Module-5	
Actuators and process control system: Introduction. Block diagram and description of process control system with an example. Introduction, Block diagram of Final control operation, Signal conversions analog, digital, pneumatic signal. Actuators, Control elements. **Electrical actuating systems:** Solid-state switches, Solenoids, Electric Motors- Principle of operation and its application: D.C motors, AC motors, Synchronous Motor, Stepper motors. **Pneumatic Actuators**: Principle and working of pneumatic actuators. (Numerical problems on the topic). **Hydraulic Actuators:** Principle and working of Hydraulic actuators. (Numerical problems on the topic).	
Teaching-Learning Process	Chalk and talk method, Power point presentation More examples relating to applications **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Discuss the fundamental concepts related to sensors and measurement, functional elements of measurement system, I/O Characteristics of measurement system.
2. Interpret and analyse the static and dynamic characteristics of instruments.
3. Elucidate the working principle and usage of different transducers for temperature, displacement and level measurement.
4. Discuss the principle and working of different types of actuators used in industrial application.
5. Discuss the principle and working of strain, force and torque measurement.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Electrical and Electronic Measurements and Instrumentation, A K Sawhney, 17th Edition, (Reprint 2004), Dhanpat Rai & Co. Pvt. Ltd., 2004.
2. Instrumentation: Devices and Systems, C S Rangan, G R Sarma, V S V Mani, 2nd Edition (32 Reprint), McGraw Hill Education (India), 2014.
3. Process Control Instrumentation Technology by C D Johnson, 7th Edition, Pearson Education Private Limited, New Delhi 2002.

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VI Semester

Artificial Neural Networks			
Course Code	**21EC641**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Preparation: To prepare students with fundamental knowledge and comprehensive understanding of artificial neural networks.
- Core Competence: To equip students to develop and configure ANNs with different types of learning algorithms for real world problems.
- Professionalism & Learning Environment: To inculcate an engineering student an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various learning algorithms.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking.
5. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1	
Introduction: Neural Networks, Application Scope of Neural Networks. **Artificial Neural Network: An Introduction**. - Fundamental Concept, Evolution of Neural Networks, Basic models of Artificial Neural Networks (ANN), Important Technologies of ANNs, McCulloch-Pitts Neuron, Linear Separability. **Text 1**: 1,1.1,1.2,2.1,2.2,2.3,2.4,2.5,2.6.	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of basic model of a neuron in comparison of biological neuron. **RBT Level:** L1, L2, L3
Module-2	
Hebb Network and simple problems **Supervised Learning Network – Introduction** –Perceptron Networks-Theory, Perceptron learning rule, architecture, flowchart for training Process, Perceptron training algorithm for single output classes, Perceptron training algorithm for Multiple output classes, Perceptron Network Testing Algorithm, Adaptive Linear Neuron- Theory, Delta rule, Architecture, flowchart, Training, Testing algorithm (Adaline), Multiple Adaptive Linear Neurons -Theory, Architecture, Flowchart, Training algorithm.	
Teaching-	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of

Learning Process	supervised learning algorithms. Problems on Hebb network **RBT Level:** L1, L2, L3

Module-3

Back–Propagation Network - Theory, Architecture, Flowchart for training process, Training Algorithm, Learning Factors of Back-Propagation Network, Testing Algorithm of Back-Propagation Network. Radial Basis Function Network, Time Delay Neural Network, Functional Link Networks.
Text 1: 3.5,3.6,3.7,3.8.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos Self-study topics: Architecture, Flowchart, Training and Testing algorithm. **RBT Level:** L1, L2, L3

Module-4

Associative Memory Network – Introduction, Training algorithm for Pattern association- Hebb Rule. Associative Memory Network - Theory, Architecture, Flowchart, Training algorithm, Testing Algorithm, Heteroassociative Memory Network- Theory, architecture, Testing algorithm, Hopfield Networks – Discrete Hopfield Network – architecture, Training algorithm, Testing algorithm of Discrete Hopfield Network.
Text 1: 4.1,4.2,4.3,4.4,4.6.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos Self-study topics: Architecture, Flowchart, Training and Testing algorithm. **RBT Level:** L1, L2, L3

Module-5

Unsupervised Learning Networks – Introduction, Fixed weight competitive nets – Maxnets, Architecture, Testing/application algorithm of Maxnet. Mexican Hat Net- Architecture, Flowchart, algorithm, Kohonen Self organizing Feature Maps – Theory, architecture. Learning Vector quantization – Theory, Architecture.
Text 1: 5.1,5.2-5.2.1,5.2.2,5.3- 5.3.1,5.3.2,5.4- 5.4.1,5.4.2.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, YouTube videos Self-study topics: Architecture, Flowchart, Training and Testing algorithm. **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Compare and contrast the biological neural network and ANN.
2. Discuss the ANN for pattern classification.
3. Develop and configure ANN's with different types of functions and learning algorithms.
4. Apply ANN for real world problems.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester

5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Book:

S N Sivanandam and S N Deepa, "Principles of Soft Computing", 2nd Edition, Wiley India Pvt. Ltd., 2014.

Reference Book:

Simon Haykin, "Neural Networks: A comprehensive foundation", 2nd Edition, PHI, 1998.

VI Semester

Cryptography			
Course Code	**21EC642**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Information Security with knowledge of mathematical concepts required for cryptography.
- Core Competence: To equip students with a basic foundation of Cryptography by delivering the basics of symmetric key and public key cryptography and design of pseudo random sequence generation technique

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different Cryptographic Techniques / Algorithms
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes
10. Give Programming Assignments

Module-1

Basic Concepts of Number Theory and Finite Fields: Divisibility and The Division Algorithm Euclidean algorithm, Modular arithmetic, Groups, Rings and Fields, Finite fields of the form GF(p), Polynomial Arithmetic, Finite Fields of the Form GF(2^m) (Text 1: Chapter 3)

Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique Programming on implementation of Euclidean algorithm, multiplicative inverse, Finite fields of the form GF(p), construction of finite field over GF(2^m). **RBT Level:** L1, L2, L3

Module-2

Introduction: Computer Security Concepts, A Model for Network Security (Text 1: Chapter 1)
Classical Encryption Techniques: Symmetric cipher model, Substitution techniques, Transposition techniques (Text 1: Chapter 1)

Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Programming on Substitution and Transposition techniques. Self-study topics: Security Mechanisms, Services and Attacks. **RBT Level:** L1, L2, L3

Module-3

Block Ciphers: Traditional Block Cipher structure, Data encryption standard (DES) (Text 1: Chapter 2: Section1, 2) The AES Cipher. (Text 1: Chapter 4: Section 2, 3, 4) **More on Number Theory**: Prime Numbers, Fermat's and Euler's theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 5)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of SDES using programming languages like C++/Python/Java/Scilab. Self-study topics: DES S-Box- Linear and differential attacks **RBT Level:** L1, L2, L3
Module-4	
ASYMMETRIC CIPHERS: Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 1, 3, 4)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of Asymmetric key algorithms using programming languages like C++/Python/Java/Scilab Numerical examples on Elliptic Curve Cryptography **RBT Level:** L1, L2, L3
Module-5	
Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16)	
Teaching-Learning Process	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of simple stream ciphers using programming languages like C++/Python/Java/Scilab. **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Explain traditional cryptographic algorithms of encryption and decryption process.
2. Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the data.
3. Apply concepts of modern algebra in cryptography algorithms.
4. Design pseudo random sequence generation algorithms for stream cipher systems.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.

Reference Books:

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

Web links and Video Lectures (e-Resources)

- https://nptel.ac.in/courses/106105031

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Programming Assignments / Mini Projects can be given to improve programming skills

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VI Semester

Python Programming			
Course Code	**21EC643**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- To learn programming using Python
- Develop application using Python

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop student's theoretical and programming skills.
2. State the need for learning Programming with real-life examples.
3. Support and guide the students for self–study.
4. You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students' progress
5. Encourage the students for group learning to improve their creative and analytical skills.
6. Show short, related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lecture activity).
   - As additional examples (post-lecture activity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution of some exercises (post-lecture activity).

Module-1

Python Basics, Python language features, History , Entering Expressions into the Interactive Shell, The Integer, Floating-Point, and String Data Types, String Concatenation and Replication, Storing Values in Variables, Your First Program, Dissecting Your Program, Flow control, Boolean Values, Comparison Operators, Boolean Operators, Mixing Boolean and Comparison Operators, Elements of Flow Control, Program Execution, Flow Control Statements, Importing Modules, Ending a Program Early with sys.exit(), Functions, def Statements with Parameters, Return Values and return Statements, The None Value, Keyword Arguments and print(), Local and Global Scope, The global Statement, Exception Handling, A Short Program: Guess the Number
Textbook 1: Chapters 1 – 3

Teaching-Learning Process	Chalk and talk method, Simulation of modulation techniques **RBT Level:** L1, L2, L3

Module-2

Data Structures: Lists: The List Data Type, Working with Lists Strings: Manipulating Strings, Working with Strings, Useful String Methods Tuples and Dictionaries, basics Using Data Structures to Model Real-World Things, Manipulating Strings.
Textbook 1: Chapters 4 – 6

Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Pattern Matching with Regular Expressions, Finding Patterns of Text Without Regular Expressions, Finding Patterns of Text with Regular Expressions, More Pattern Matching with Regular Expressions,, The findall() Method, Character Classes, Making Your Own Character Classes, The Caret and Dollar Sign Characters, The Wildcard Character, Review of Regex Symbols. Reading and Writing Files, Files and File Paths, The os.path Module, The File Reading/Writing Process, Saving Variables with the shelve Module, Saving Variables with the pprint. pformat() Function Textbook 1: Chapters 7, 8	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation **RBT Level:** L1, L2, L3
Module-4	
Classes and objects: Programmer-defined types, Attributes, Rectangles, Instances as return values, Objects are mutable, Copying, Classes and functions: Time, Pure functions, Modifiers, Prototyping versus planning, Classes and methods: Object-oriented features, Printing objects, Another example, The init method, The__str__ method, Operator overloading, Type-based dispatch, Polymorphism. Textbook 2: Textbook 2: Chapters 15 – 18	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation **RBT Level:** L1, L2, L3
Module-5	
HTTP, The World's simplest Web Browser, Retrieving an image over HTTP, Retrieving web pages with urllib, Parsing html and scraping the web, Parsing HTML using RE, BeautifulSoup, Reading binary files using urllib, XML, Parsing XML, Looping through nodes, JSON, Parsing JSON, API, geocoding Web Service, Security & API usage, What is database?, Database Concepts, Database Browser, Creating a database table, SQL, Spidering Twitter, Basic data modeling, Programming with multiple tables, Three kinds of Keys, JOIN Text book : Chapter 2, 13, 15	
Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. To acquire programming skills in Python
2. To demonstrate data structure representation using Python
3. To develop the skill of pattern matching and files in Python
4. To acquire Object Oriented Skills in Python
5. To develop the ability to write database applications in Python

Assessment Details (both CIE and SEE)

The weightage of Continuous 5 End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Al Sweigart, "Automate the Boring Stuff with Python",1st Edition, No Starch Press, 2015. (Available under CC-BY-NC-SA license at https://automatetheboringstuff.com/) (Chapters 1 to 8)
2. Allen B Downey, "Think Python: How to Think Like a Computer Scientist", 2nd Edition, Green Tea Press, 2015. (Available under CC-BY-NC license at http://greenteapress.com/thinkpython2/thinkpython2.pdf) (Chapters 15 - 18) (Download pdf/html files from the above links)
3. Charles R. Severance, "Python for Everybody: Exploring Data Using Python 3", 1st, Create Space Independent Publishing Platform, 2016

Web links and Video Lectures (e-Resources)

- https://www.youtube.com/watch?v=_xQNeOTRyig
- https://www.youtube.com/watch?v=kqtD5dpn9C8

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Write a program to generate Fibonacci series
- Write a program to find factorial of a number using function.
- Write a menu driven program to implement stack using Lists
- Create a DB using dictionaries containing key as USN and related fields containing Name, gender, Marks1, Marks2 & Marks3 of students. Implement the following functions to perform i) Update Name/gender/marks ii) search for usn and display the relevant fields iii) delete based on search for name iv)generate the report with avg marks more than 70%
- Write a program to implement search and replace multiple occurrences of a given substring in the main string in a list.
- Write a function called most_frequent that takes a string and prints the letters in decreasing order of frequency.
- Write a program that reads a file, display the contents, builds a histogram of the words in the file and print most common words in the file.
- Write a program that searches a directory and all of its subdirectories, recursively, and returns a list of complete paths for all files with a given suffix.

03.10.2022

- Write python code to extract From: and To: Email Addresses from the given text file using regular expressions. https://www.py4e.com/code3/mbox.txt.
- Consider the sentence *"From rjlowe@iupui.edu Fri Jan 4 14:50:18 2008",* Write python code to extract email address and time of the day from the given sentence
- Write a program to read, display and count number of sentences of the given file.
- Write a program that gets the current date and prints the day of the week.
- Write a function called print_time that takes two Time objects and prints total time it in the form hour:minute:second.
- Write a program that takes a birthday as input and prints the user's age and the number of days, hours, minutes and seconds until their next birthday.

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VI Semester

Micro Electro Mechanical Systems			
Course Code	**21EC644**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3: 0 :0 : 1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- **Preparation**: To prepare students with fundamental knowledge/ overview in the field of Micro Electro Mechanical Systems.
- **Core Competence**: To equip students with a basic foundation in electronic engineering, mechanical engineering, electrical engineering, chemistry, physics and mathematics fundamentals required for comprehending the operation and application of MEMS circuits, design.
- **Professionalism & Learning Environment:** To inculcate in students an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.

Teaching-Learning Process (General Instructions)
These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes
2. Show Video/animation films to explain the functioning of various
3. Encourage collaborative (Group) Learning in the class to promote critical thinking
4. Topics for seminars on several MEMS related topics and their applications
5. Encourage the students to take up mini projects and main projects
6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.
Text1: **1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8, 1.9**

Teaching-Learning Process	Chalk and talk method, Animation of MEMS products and applications **RBT Level:** L1, L2, L3

Module-2

Working Principles of Microsystems: Introduction, Microsensors, Micro actuation, MEMS with Micro actuators, Micro accelerometers, Microfluidics. **Text1: 2.1,2.2, 2.3, 2.4, 2.5, 2.6**
Engineering Science for Microsystems Design and Fabrication: Introduction, Atomic Structure of Matter, Ions and Ionization Molecular Theory of Matter and Intermolecular Forces, Plasma Physics, Electrochemistry. **Text1: 3.1, 3.2, 3.3, 3.4, 3.7, 3.8**

Teaching-Learning Process	PowerPoint Presentation, YouTube videos, Animations of MEMS Micro sensors, Micro actuators, Micro accelerometers and Microfluidics, molecules, Ions and matter **RBT Level:** L1, L2, L3

Module-3	
Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermo mechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis. **Text1: 4.1,4.2,4.3,4.4,4.5,4.6,4.7**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentations and supporting YouTube Videos Solve numericals related to Thin Plates, and Vibration. Self study topics: solve numericals related to other topics **RBT Level:** L1, L2, L3
Module-4	
Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling in Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer. **Text1: 6.1, 6.2,6.3,6.4,6.5,6.6,6.7,6.8**	
Teaching-Learning Process	Chalk and Talk Method, You Tube Videos, Solve numericals related to scaling in Geometry Self study topics: solve numericals of other topics **RBT Level:** L1, L2, L3
Module-5	
Overview of Micromanufacturing: Introduction, Bulk Micromanufacturing, Surface Micromachining, The LIGA Process, Summary on Micromanufacturing. **Text1: 9.1,9.2,9.3,9.4,9.5** **Microsystem Packaging**: Introduction, Overview of Mechanical Packaging of Microelectronics, Microsystem Packaging. **Text1: 11.1,11.2, 11.3**	
Teaching-Learning Process	Power Point Presentation, YouTube videos, Animation of MEMS micromanufacturing Supporting animation videos on packaging **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Appreciate the technologies related to Micro Electro Mechanical Systems.
2. Understand design and fabrication processes involved with MEMS devices.
3. Analyse the MEMS devices and develop suitable mathematical models
4. Know various application areas for MEMS device.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Book:

Tai-Ran Hsu, MEMS and Micro systems: Design and Manufacture, 1st Ed, Tata Mc Graw Hill.

Reference Books:

1. **Hans H Gatzen, Volker Saile, JurgLeuthold**, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. **Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik**, Microelectromechanical Systems (MEMS), Cengage Learning.
3. **Chang Liu**, Foundations of MEMS, Pearson Ed.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Develop mini projects and Final year projects using MEMS components to address the real world problems

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VII Semester

Advanced VLSI			
Course Code	**21EC71**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Learn overview of VLSI design flow
- Emphasise on Back end VLSI design flow
- Learn basics of verification with reference to System Verilog

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. CMOS Logic: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers. Text Book 1

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.
Routing: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back annotation. Text Book 1

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components, layered testbench. **Data Types**: Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a type, creating new types with type def, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width. Text Book 2	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Procedural Statements and Routines: Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values. **Connecting the test bench and design**: Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions. Text Book 2	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Randomization: Introduction, What to randomize? , Randomization in System Verilog, Random number functions, Common randomization problems, Random Number Generators. **Functional Coverage**: Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation. Text Book 2	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand VLSI design flow
2. Describe the concepts of ASIC design methodology
3. Create floor plan including partition and routing with the use of CAD algorithms
4. Will have better insights into VLSI back-end design flow
5. Learn verification basics and System Verilog

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Michael John Sebastian Smith, Application - Specific Integrated Circuits, Addison-Wesley Professional, 2005.
2. Chris Spear, System Verilog for Verification – A guide to learning the Test bench language features, Springer Publications, Second Edition, 2010.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Use EDA tool to design basic Analog blocks like amplifiers and 4-bit RAM
- Prepare a white paper on ASIC design flow referring to literatures of Cadence and Synopsys EDA tools
- Mini project using System Verilog

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VII Semester

Optical & Wireless Communication			
Course Code	**21EC72**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:0:0:1	SEE Marks	50
Total Hours of Pedagogy	30	Total Marks	100
Credits	2	Exam Hours	3

Non-MCQ pattern of CIE and SEE

Course objectives:

This course will enable students to:

- Learn the basic principle of optical fiber communication with different modes of light propagation.
- Understand the transmission characteristics and losses in optical fiber.
- Study of optical components and its applications in optical communication networks.
- Understand the concepts of propagation over wireless channels from a physics standpoint
- Understand the multiple access techniques used in cellular communications standards.
- Application of Communication theory both Physical and networking to understand GSM systems that handle mobile telephony.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Optical Fiber Structures: Optical Fiber Modes and Configurations, Mode theory for circular waveguides, Single mode fibers, Fiber materials.

Attenuation and Dispersion: Attenuation, Absorption, Scattering Losses, Bending loss, Signal Dispersion: Modal delay, Group delay, Material dispersion.

[Text1 : 3.1, 3.2, 2.3[2.3.1 to 2.3.4], 2.4[2.4.1, 2.4.2],2.5, 2.7].

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

Optical Sources and detectors: Light Emitting Diode: LED Structures, Light source materials, Quantum efficiency and LED power, Laser Diodes: Modes and threshold conditions, Rate equations, External quantum efficiency, Resonant frequencies, Photodetectors: The pin Photodetector, Avalanche Photodiodes.

WDM Concepts: Overview of WDM, Isolators and Circulators, Fiber grating filters, Dielectric thin-film filters, Diffraction Gratings. [Text1: 4.2 ,4.3, 6.1, 10.1, 10.3, 10.4, 10.5, 10.7]	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-3	
Mobile Communication Engineering: Wireless Network generations, Basic propagation Mechanisms, Mobile radio Channel. **Principles of Cellular Communications:** Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Frequency Reuse Distance, Cochannel Interference and signal quality. [Text2: 1.4, 2.4, 2.5, 4.1 to 4.4, 4.6, 4.7]	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Multiple Access Techniques: FDMA, TDMA, CDMA, SDMA, Hybrid Multiple Access Techniques, Multicarrier Multiple Access Schemes. **A Basic Cellular System:** A basic cellular system connected to PSTN, Parts of basic cellular system, Operation of a cellular system. [Text2: 8.2, 8.3, 8.4.5, 8.5, 8.6, 8.10, 9.2.2, 9.2.3, 9.3]	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Global System for Mobile (GSM): GSM Network Architecture, GSM signalling protocol architecture, Identifiers used in GSM system, GSM Channels, Frame structure for GSM, GSM Call procedures, GSM hand-off Procedures, GSM Services and features. [Text2: 11.1, 11.2,11.3,11.4, 11.5, 11.8, 11.9. 11.10]	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Classification and characterization of optical fibers with different modes of signal propagation.
2. Describe the constructional features and the characteristics of optical fiber and optical devices used for signal transmission and reception.
3. Understand the essential concepts and principles of mobile radio channel and cellular communication.
4. Describe various multiple access techniques used in wireless communication systems.
5. Describe the GSM architecture and procedures to establish call set up, call progress handling and call tear down in a GSM cellular network.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation (CIE):

CIE will be the same as other core theory courses.

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.
Semester End Examination (SEE):

For non-MCQ pattern of CIE and SEE

Continuous Internal Evaluation (CIE):

At the beginning of the semester, the instructor/faculty teaching the course has to announce the methods of CIE for the course.

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books

1. Gerd Keiser, Optical Fiber Communication, 5th Edition, McGraw Hill Education (India) Private Limited, 2016. ISBN:1-25-900687-5.
2. T L Singal, Wireless Communications, McGraw Hill Education (India) Private Limited, 2016, ISBN:0-07-068178-3.

Reference Books

1. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3
2. Theodore Rappaport, Wireless Communications: Principles and Practice, 2nd Edition, Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0-13-042232-0.
3. Gary Mullet, Introduction to Wireless Telecommunications Systems and Networks, First Edition, Cengage Learning India Pvt Ltd., 2006, ISBN - 13: 978-81-315-0559-5.

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VII Semester

Optical & Satellite Communication			
Course Code	**21EC741**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to:

- Learn the basic principle of optical fiber communication with different modes of light propagation.
- Understand the transmission characteristics and losses in optical fiber.
- Study of optical components and its applications in optical communication networks.
- Understand the basic principle of satellite orbits and trajectories.
- Study of electronic systems associated with a satellite and the earth station.
- Study satellite applications focusing various domains services such as remote sensing, weather forecasting and navigation.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Optical Fiber Structures: Optical Fiber Modes and Configurations, Mode theory for circular waveguides, Single mode fibers, Fiber materials, Photonic Crystal Fibers, Fiber Optic Cables.
Attenuation and Dispersion: Attenuation: Absorption, Scattering Losses, Bending loss, Signal Dispersion: Modal delay, Group delay, Material dispersion.
[Text1 : 2.3[2.3.1 to 2.3.4], 2.4[2.4.1, 2.4.2],2.5, 2.7,2.8, 2.11, 3.1, 3.2].

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. Self-study topics: Optical Spectral bands, Basic optical laws and definitions. **RBT Level:** L1, L2, L3

Module-2

Optical Sources and detectors: Light Emitting Diode: LED Structures, Light source materials, Quantum efficiency and LED power, Laser Diodes: Modes and threshold conditions, Rate equations, External quantum efficiency, Resonant frequencies, Photodetectors: The pin Photodetector, Avalanche Photodiodes.
WDM Concepts: Overview of WDM, Isolators and Circulators, Fiber grating filters, Dielectric thin-film filters, Diffraction Gratings.

Optical Amplifiers: Basic Applications and types, Erbium doped fiber amplifiers. [Text1: 4.2 ,4.3, 6.1, 10.1, 10.3, 10.4, 10.5, 10.7, 11.1, 11.3.1,11.3.2]	
Teaching-Learning Process	Chalk and talk method, Power point presentation Self-study topics: Raman Amplifiers. **RBT Level:** L1, L2, L3
Module-3	
Satellite Orbit and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits. [Text2: 2.1, 2.2, 2.3,2.4,2.5] **Satellite In-orbit Operations:** Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle. [Text2: 3.3, 3.4, 3.5, 3.6, 3.7]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. Self-study topics: Satellite launch sequence. **RBT Level:** L1, L2, L3
Module-4	
Satellite Hardware: Satellite Subsystems, Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload. [Text2: 4.1, 4.5, 4.6, 4.7,4.8] **Earth Station:** Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking. [Text2: 8.1, 8.2, 8.3,8.4,8.5,8.6]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. Self-study topics: Mechanical structure and propulsion subsystem **RBT Level:** L1, L2, L3
Module-5	
Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Television, Satellite Data Communication Services. **Applications:** Remote Sensing Satellites: Classification, Orbits, payloads. Weather Forecasting Satellites: Overview, Fundamentals, orbits and payload. Global Positioning Satellite System.	
Teaching-Learning Process	Chalk and talk method, Power point presentation Self-study topics: Regional, National and International Satellite systems **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Classification and characterization of optical fibers and devices used for optical communication.
2. Understand the principle of operation of optical devices used for multiplexing and amplification of light.
3. Describe the satellite orbits and its trajectories with the definitions of parameters associated with it.
4. Describe the electronic hardware systems associated with the satellite subsystem and earth station.
5. Understand the functioning of satellites for communication, remote sensing, and weather and navigation applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester

2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Gerd Keiser, Optical Fiber Communication, 5th Edition, McGraw Hill Education (India) Private Limited, 2016. ISBN:1-25-900687-5.
2. Anil K Maini, Varsha Agrawal, Satellite Communication, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

Reference Books:

1. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4
3. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006.

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VII Semester

ARM Embedded Systems			
Course Code	**21EC742**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

This course will enable students to:

- Explain the architectural features and instructions of 32 bit ARM microcontroller
- Develop Programs using the various instructions of ARM for different Applications.
- Understand the basic hardware components and their selection method based on the characteristics and
- Attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
8. Give programming assignments.

Module-1

ARM Embedded System: RISC Design Philosophy, ARM design Philosophy, Embedded System hardware and Embedded System software.
ARM Processor Fundamentals: Registers, Current Program Status Registers, Pipeline, Exceptions, Interrupts and the Vector table, Core Extensions, Architecture Revisions, ARM processor families
(Text1 : Chapter 1 and Chapter 2)

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

ARM Instructions: Introduction, Data Processing Instructions, Branch Instructions, Load – Store Instructions Software Instructions, Program Status Register Instructions, Conditional Execution.
Thumb Instructions: Thumb register usage, ARM – Thumb Interworking, Other branch Instructions, Data Processing instructions, Single and Multiple Register Load Store Instructions, Stack Instructions, Software Interrupt Instructions.
(Text1: Chapter 3 and chapter 4,)

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3

Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Elements of an Embedded System (Block diagram and explanation), Differences between RISC and CISC, Harvard and Princeton, Big and Little Endian formats, Memory (ROM and RAM types), Sensors, Actuators, Optocoupler, Communication Interfaces (I2C, SPI, IrDA, Bluetooth, Wi-Fi, Zigbee only)

(Text 2: All the Topics from Ch-1 and Ch-2 (Fig and explanation before 2.1) 2.1.1.6 to 2.1.1.8, 2.2 to 2.2.2.3, 2.3 to 2.3.2, 2.3.3.3, selected topics of 2.4.1 and 2.4.2 only).

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-4

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language).
Text 2: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-5

RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques
(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch-12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
2. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
3. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
4. Develop the hardware software co-design and firmware design approaches.
5. Explain the need of real time operating system for embedded system applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Andrew N Sloss, "ARM System Developer's guide", Elsevier Publications, 2016
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2nd Edition.

Reference Books:

1. James K Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.
2. Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", 2nd Ed., Man Press LLC ©, 2015.
3. K V K K Prasad, "Embedded real time systems", Dreamtech publications, 2003.
4. Rajkamal, "Embedded Systems",2nd Edition, McGraw hill Publications, 2010.

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VII Semester

Basic Digital Image Processing			
Course Code	**21EC743**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:0:2:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Understand the fundamentals of digital image processing
- Understand the image enhancement techniques in spatial domain used in digital image processing
- Understand the frequency domain enhancement techniques in digital image processing
- Understand the Color Image Processing in digital image processing
- Understand the image restoration techniques and methods used in digital image processing

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Show Video/animation films to explain the functioning of various image processing concepts.
2. Encourage cooperative (Group) Learning through puzzles, diagrams, coding etc., in the class.
3. Encourage students to ask questions and investigate their own ideas helps improve their problem-solving skills as well as gain a deeper understanding of academic concepts.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Students are encouraged to do coding based projects to gain knowledge in image processing.
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Arrange visits to nearby PSUs such as CAIR(DRDO), NAL, BEL, ISRO, etc., and small-scale software industries to give industry exposure.

Module-1

Digital Image Fundamentals: What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels.
[Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on Image processing applications Self-study topics: Arithmetic and Logical operations Practical topics: Problems on Basic Relationships Between Pixels. **RBT Level:** L1, L2, L3

Module-2

Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters
[Text 1: Chapter 3: Sections 3.2 to 3.6]

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos and animations of Intensity Transformation Functions, Histogram Processing, Spatial domain filters. Self-study topics: Point, line and edge detection. Practical topics: Problems on Intensity Transformation Functions, Histogram, Spatial domain filters **RBT Level:** L1, L2, L3

Module-3

Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters.

[Text 1: Chapter 4: Sections 4.7 to 4.9]

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos on frequency domain filtering, Color image processing. Self-study topics: Basic concept of segmentation. Practical topics: Problems on Image smoothing and sharpening **RBT Level:** L1, L2, L3

Module-4

Color Image Processing: Color Fundamentals, Color Models, Pseudo-color Image Processing.

[Text 1: Chapter 6: Sections 6.1 to 6.3]

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos on Color image processing. Practical topics: Problems on Pseudo-color Image Processing **RBT Level:** L1, L2, L3

Module-5

Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering.

[Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8]

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos on Noise models, filters and its applications. Self-study topics: Linear position invariant degradation, Estimation of degradation function. **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Understand image formation and the role of human visual system plays in perception of gray and color image data.
2. Apply image processing techniques in spatial domains.
3. Apply image processing techniques in frequency (Fourier) domains.
4. Conduct independent study and analysis of Image Enhancement techniques.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester

3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Book:

Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3rd Edition, 2010.

Reference Books:

1. Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.
2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.

Web links and Video Lectures (e-Resources)

- Image databases, https://imageprocessingplace.com/root_files_V3/image_databases.htm
- Student support materials, https://imageprocessingplace.com/root_files_V3/students/students.htm
- NPTEL Course, Introduction to Digital Image Processing, https://nptel.ac.in/courses/117105079
- Computer Vision and Image Processing, https://nptel.ac.in/courses/108103174
- Image Processing and Computer Vision – Matlab and Simulink,
- https://in.mathworks.com/solutions/image-video-processing.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Simulink models for Image processing

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VII Semester

Basic Digital Signal Processing			
Course Code	**21EC744**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

This course will enable students to:

- **Preparation**: To prepare students with fundamental knowledge/ overview in the field of Signal Processing
- **Core Competence**: To equip students with a basic foundation of Signal Processing by delivering the mathematical description of discrete time signals and systems, classifying signals into different categories based on their properties, analyzing Linear Time Invariant (LTI)systems in time and transform domains, basics of FIR & IIR Filter Design

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts Digital Signal Processing.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes
10. Give Programming Assignments.

Module-1

Signal Definition, Signal Classification, System definition, System classification, for both continuous time and discrete time, Definition of LTI systems (Chapter1)

Teaching-Learning Process	Chalk and talk method, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-2

Introduction to Fourier Transform, Fourier Series, Relating the Laplace Transform to Fourier Transform, Frequency response of continuous time systems (Chapter3)

Teaching-Learning Process	Chalk and talk method, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Module-3	
Frequency response of ideal analog filters, Salient features of Butterworth filters Design and implementation of Analog Butterworth filters to meet given specifications (Chapter8)	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3
Module-4	
Sampling Theorem- Statement and proof, converting the analog signal to a digital signal, Practical sampling, The Discrete Fourier Transform, Properties of DFT, Comparing the frequency response of analog and digital systems (FFT not included) (Chapter 3,4)	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3
Module-5	
Definition of FIR and IIR filters, Frequency response of ideal digital filters. Transforming the Analog Butterworth filter to the Digital IIR Filter using BLT to meet given specifications. Design of Low pass / High pass FIR Filters using the Window technique, to meet given specifications, Comparing the designed filter with the desired filter frequency response (Chapter8)	
Teaching-Learning Process	Chalk and talk method, Power point presentation, YouTube videos, Flipped Class Technique, Programming assignments **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the continuous time and discrete time signals and systems, in time and frequency domain
2. Apply the concepts of signals and systems to obtain the desired parameter/representation
3. Design analog/digital filters to meet given specifications
4. Design and implement the analog filter using components/suitable simulation tools
5. Design and implement the digital filter (FIR/IIR) using suitable simulation tools, and record the input and output of the filter for the given audio signal

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. 'Signals and Systems', Simon Haykin and Barry Van Veen, Wiley.
2. "Fundamentals of Digital Signal Processing", Lonnie C Ludeman, John Wiley and Sons, 1986.

Reference Books:

3. 'Theory and Application of Digital Signal Processing', Rabiner and Gold
4. 'Signals and Systems', Schaum's Outline series
5. 'Digital Signal Processing', Schaum's Outline series

Web links and Video Lectures (e-Resources)

By Prof. S C Dutta Roy, IIT Delhi
https://nptel.ac.in/courses/117102060

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Programming Assignments / Mini Projects can be given to improve programming skills

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VII Semester

E-waste Management			
Course Code	**21EC745**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- **Current Status:** According to a report on e-waste presented by the United Nations (UN) in World Economic Forum on January 24, 2019, the waste stream reached 48.5 MT in 2018. With such a large quantity of e-waste being generated each year, the future of e-waste recycling in India looks pretty bright. The E-waste (Management) Rules, 2016, enacted on October 1, 2017, added over 21 products (Schedule-I) under the purview of the rule.
- **Purview:** This course covers an extensive review of e-waste management in India. With a focus on the evolution of legal frameworks in India and the world, it presents impacts and outcomes; challenges and opportunities; and management strategies and practices to deal with e-waste. It also includes a survey of pan-India initiatives and trajectories of law-driven initiatives for effective e-waste management along with responses from industries and producers.
- **Scope:** There is a considerable scope for e-waste recycling in India. It is not only a solution to help mitigate e-waste management issues, but it also helps to generate employment. With the rise in e-waste recycling plants, the demand for employees with all levels of qualification and skills also increases.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps to improve the students' understanding.
8. Arrange visits to nearby industries to give industry exposure.

Module-1

Sustainable development and e-waste management: Importance of electrical and electronic equipment in a nation's development, and e-waste as toxic companion of digital era, I: Let's understand e-waste, II: E-waste statistics: quantities, collection and recycling, E-waste categories and harmonising statistics, III: An overview on status of e-waste related legislation across the globe; IV: UN initiatives for e-waste management: creating partnerships and achieving Agenda 2030; V: Indian scenario: e-waste generation, collection and recycling.

Teaching-Learning Process	Chalk and talk method, YouTube videos. **RBT Level:** L1, L2

Module-2

Extended producer responsibility: a mainstay for e-waste management: Evolution of concept of 'extended producer responsibility', EPR applied for waste management and extended for e-waste

management, EPR: goals, implementation, and challenges for e-waste management, EPR implemented for e-waste management under the existing regulatory frameworks in different countries, Role of a PRO prescribed in regulatory framework, Considerations for successful implementation of EPR, Challenges in implementation of EPR for e-waste management, Impact of EPR, EPR and e-waste management in India. **Toxicity and impacts on environment and human health**: Toxicity, recycling, and regulations, I: Environmental concerns, II: Human health concerns.	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, More examples relating to applications. **RBT Level:** L1, L2, L3
Module-3	
Treating e-waste, resource efficiency, and circular economy: Safe environment, resource use, and circular economy, Circular economy: recycling, resource recovery, and resource efficiency, Potentials of urban mining in circular economy, Recycling and resource efficiency related challenges to the circular economy, Urban mining, recycling, resource use, resource efficiency, and circular economy in India. **E-waste management through legislations in India**: I: Historical backdrop of regulatory regime for e-waste in India, II: E-waste (management) Rules, 2016 and E-waste (management) Amendment Rules, 2018, III: Analysing performance of EPR and CPCB as regulatory mechanisms, IV: Legal cases and judicial directives.	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation **RBT Level:** L1, L2, L3
Module-4	
Strategies and initiatives for dealing with e-waste in India: I: Overview of pan-India initiatives for dealing with e-waste during 2000 and 2012, II: Law-driven e-waste management – initiatives by the government, non-government agencies, and judiciary.	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation. **RBT Level:** L1, L2, L3
Module-5	
Moving towards horizons: I: Legal and judicial domain, II: Economic concerns, III: Environment concerns, IV: Recycling culture/recycling society.	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, More examples relating to applications. **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the existing discourse on e-waste and its management, statistics across the world, opportunities, and challenges w.r.t. regulatory framework, SDGs, CE, and LCIA (Life Cycle Impact Assessment) and MFA (Material Flow Analysis), Indian scenario.
2. Describe EPR, a regulatory framework for achieving specified goals across different countries and impacts on environment and human health.
3. Explain themes in the context of resource use and sustainable development. Urban mining, informal sector operations and need for resource use policy, financial support for recycling infrastructure building, etc. in Indian context and also explain to what extent – different aspects of e-waste management have been incorporated in the existing regulatory framework in comparison with international legislatures.
4. Identify and infer pan-Indian initiatives dealing with e-waste management, ranging from building knowledge base through research and social action by different stakeholders to technological and legal advancements, and industrial initiatives. Analyse roadmap for the Agenda 2030.
5. Use opportunities and challenges around four domains: legal and judicial domain; economic concerns; recycling culture/society; and environment concerns.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Book:

Varsha Bhagat Gangulay, 'E-Waste Management', Taylor and Francis, 2022.

Web links and Video Lectures (e-Resources)

•https://link.springer.com/book/10.1007/978-3-030-14184-4
•https://rajyasabha.nic.in/rsnew/publication_electronic/E-Waste_in_india.pdf
•https://greene.gov.in/wp-content/uploads/2018/01/E-waste-Vol-II-E-waste-Management-Manual.pdf
•https://nptel.ac.in/courses/105105169

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

• Groups can be made to conduct a survey on the present scenario of India and top 5 countries facing ewaste management challenges.
• Industry visits to give an exposure of the e waste management process and also business.
• Case studies to develop e-waste management models.
• Survey of few e-waste management companies can be carried out and submit report.

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VII Semester

Advanced Design Tools for VLSI			
Course Code	**21EC721**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Impart knowledge of EDA tools and methodology for FPGA
- Learn principles of IP core for FPGA and embedded systems
- Infer the concept of machine learning in fabrication and physical design

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Arrange visits to nearby PSUs and small-scale communication industries.
3. Show Video/animation films to explain the functioning of various techniques.
4. Encourage collaborative (Group) Learning in the class
5. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
9. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: Introduction, Prologue, EDA: From Methodologies, Algorithms, Tools to Integrated Circuits and Systems, EDA from Halcyon's Days to the Blooming Paradigm of Chip Industry, Categories of the EDA Tools, Quo Vadis, EDA? The Challenges and Opportunities, Designing the System as SoC Using the Soft IP Cores, Types of IP Cores, Design Issues Pertaining to the Soft IP Cores
Text Book1: 1.1 to 1.5, 1.7 to 1.10

Development of FPGA Based Network on Chip for Circumventing Spam: Introduction, Conception of the Spam Mail, FPGA Based Network on Chip for Circumventing Spam, Tools Infrastructure and Design Flow, Introducing Hardware-Software Co-design, Hardware Software Co-design, Framework Proposed in the Present Case Study, Description of System at Higher Level, Resolving the System a Step Down, System Design, Development of Soft IP Core of Bloom Filter, Presenting System Design of Purely Software Modules, Integrating of the Hardware-Software Modules Using EDK
Text Book1: 2.1 to 2.13

Teaching-Learning Process	Chalk and talk method, , PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2, L3

Module-2

Analog Front End and FPGA Based Soft IP Core for ECG Logger: Prior Art, The Very Rationale of the System, Analog Front End of the Setup, VHDL Implementation of the ECG Soft IP Core, ModelSim Simulation Results, Synthesis Results Using Mentor Graphics Tool, Monitoring the ECG Using MODEM

Based Setup, ECG Signal Reconstruction Mechanism at the Hospital End, VHDL Listing for Driving the Analog Demultiplexer and Serial DAC from Spartan-3E FPGA, Discussion Regarding the VHDL Implementation, ModelSim Simulation Results, Synthesis Results Using Mentor Graphics Tool: Leonardo Spectrum. Text Book1: 3.1 to 3.12	
Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3
Module-3	
FPGA Based Multifunction Interface for Embedded Applications: Introduction, Universal FPGA Based Interface for High End Embedded Applications, Soft IP Core for the LCD Interface, Soft IP Core for the DAC Interface, Handel C Listing of the Soft IP Core for the DAC Interface, Soft IP Core for the Linear Tech LTC6912-1 Dual Amp, Soft IP Core for the ADC Interface, Soft IP Core for the VGA Interface, Soft IP Core for the Keyboard Interface, Triangular Wave Generator Using DAC Text Book1: 4.1 - 4.10	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Machine Learning for Compact Lithographic Process Models: Introduction, The Lithographic Patterning Process, Machine Learning of Compact Process Models, Neural Network Compact Patterning Models. Text Book2: 2.1 to 2.4 **Machine Learning for Mask Synthesis**: Introduction, Machine Learning-Guided OPC, Machine Learning-Guided EPC. Text Book2: 3.1 to 3.4	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Machine Learning in Physical Verification, Mask Synthesis, and Physical Design: Introduction, Machine Learning in Physical Verification, Machine Learning in Mask Synthesis, Machine Learning in Physical Design. Text Book2: 4.1 to 4.4	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Demonstrate the EDA methodologies and Tools for FPGA based NoC
2. Interpretation of soft core for ECG logger
3. Interfacing of DAC for embedded Application
4. Interpretation of Machine Learning for fabrication
5. Interpretation of ML in physical design

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester

2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Rajanish K Kamat, Santosh A Shinde, Pawan K Gaikwad, Hansraj Guhilot, 'Harnessing VLSI System Design with EDA Tools', Springer, 2012.
2. Ibrahim (Abe) M Elfadel, Duane S Boning, Xin Li, 'Machine Learning in VLSI Computer-Aided Design', Springer, 2011.

Web links and Video Lectures (e-Resources)

- https://www.digimat.in/nptel/courses/video/117101004/L01.html
- https://www.youtube.com/watch?v=zC5b5_7oRKk

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VII Semester

Digital Image Processing			
Course Code	**21EC722**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Understand the fundamentals of digital image processing.
- Understand the image transform used in digital image processing.
- Understand the image enhancement techniques in spatial domain used in digital image processing.
- Understand the Color Image Processing and frequency domain enhancement techniques in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Show Video/animation films to explain the functioning of various image processing concepts.
2. Encourage cooperative (Group) Learning through puzzles, diagrams, coding etc., in the class.
3. Encourage students to ask questions and investigate their own ideas helps improve their problem-solving skills as well as gain a deeper understanding of academic concepts.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Students are encouraged to do coding based projects to gain knowledge in image processing.
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding
9. Arrange visits to nearby PSUs such as CAIR (DRDO), NAL, BEL, ISRO, etc., and small-scale software industries to give industry exposure.

Module-1

Digital Image Fundamentals: What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels.
[Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on Image processing applications Self-study topics: Arithmetic and Logical operations Practical topics: Problems on Basic Relationships Between Pixels. **RBT Level:** L1, L2, L3

Module-2	
Image Transforms: Introduction, Two-Dimensional Orthogonal and Unitary Transforms, Properties of Unitary Transforms, Two-Dimensional DFT, cosine Transform, Haar Transform. Text 2: Chapter 5: Sections 5.1 to 5.3, 5.5, 5.6, 5.9]	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos of various transformation techniques and related applications. Self-study topics: Sine transforms, Hadamard transforms, KL transform, Slant transform. Practical topics: Problems on DFT and DCT **RBT Level:** L1, L2, L3
Module-3	
Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters [Text: Chapter 3: Sections 3.2 to 3.6]	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos and animations of Intensity Transformation Functions, Histogram Processing, Spatial domain filters. Self-study topics: Point, line and edge detection. Practical topics: Problems on Intensity Transformation Functions, Histogram, Spatial domain filters **RBT Level:** L1, L2, L3
Module-4	
Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters. **Color Image Processing:** Color Fundamentals, Color Models, Pseudo-color Image Processing. [Text 1: Chapter 4: Sections 4.7 to 4.9 and Chapter 6: Sections 6.1 to 6.3]	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos on frequency domain filtering, Color image processing. Self-study topics: Basic concept of segmentation. Practical topics: Problems on Pseudo-color Image Processing **RBT Level:** L1, L2, L3
Module-5	
Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering. [Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8]	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos on Noise models, filters and its applications. Self-study topics: Linear position invariant degradation, Estimation of degradation function. **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand image formation and the role of human visual system plays in perception of gray and color image data.
2. Compute various transforms on digital images.
3. Conduct independent study and analysis of Image Enhancement techniques.
4. Apply image processing techniques in frequency (Fourier) domain.
5. Design image restoration techniques.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3rd Edition 2010.
2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.

Reference Book:

Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.

Web links and Video Lectures (e-Resources)

- Image databases, https://imageprocessingplace.com/root_files_V3/image_databases.htm
- Student support materials, https://imageprocessingplace.com/root_files_V3/students/students.htm
- NPTEL Course, Introduction to Digital Image Processing, https://nptel.ac.in/courses/117105079
- Computer Vision and Image Processing, https://nptel.ac.in/courses/108103174
- Image Processing and Computer Vision – Matlab and Simulink,
- https://in.mathworks.com/solutions/image-video-processing.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Verilog /VHDL coding for Image manipulation.
- Simulink models for Image processing.

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VII Semester

DSP Algorithms & Architecture			
Course Code	**21EC723**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

This course will enable the students to

- Understand the concepts of digital signal processing techniques.
- Understand the computational building blocks of DSP processors and its speed issues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of the TMS320C54xx processor.
- Learn how to interface the external devices to the TMS320C54xx processor in various modes.
- Understand DSP algorithms and applications with their implementation using TMS320C54xx processor.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Digital Signal Processing: Introduction, A Digital Signal – Processing system, Major features of programmable Digital signal processors, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.
Section 1.3, 2.1 to 2.8 of Text 1

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

Architectures for Programmable Digital Signal Processing Devices: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.
Section 4.1 to 4.9 of Text 1

Teaching-Learning	Chalk and talk method, Power point presentation

Process	**RBT Level:** L1, L2, L3
Module-3	
Programmable Digital Signal Processors: Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor. Section 5.1 to 5.10 of Text 1	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Implementation of Basic DSP Algorithms: Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). **Implementation of FFT Algorithms**: Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx. Section 7.1 to 7.6 and 8.1 to 8.6 of Text 1	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices: Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA). **Interfacing and Applications of DSP Processors**: Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System. Section 9.1 to 9.8, 10.1 to 10.5 and11.1 to 11.5 of Text 1	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Comprehend the knowledge & concepts of digital signal processing techniques.
2. Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.
3. Develop assembly language programs to implement FIR, IIR filters and FFT algorithms.
4. Build the Applications on Programmable DSP devices.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20**

Marks (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Book:

"Digital Signal Processing", Avatar Singh and S Srinivasan, Thomson Learning, 2004

Reference Books:

1. "Digital Signal Processing: A practical approach", Ifeachor E C, Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd Ed., 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch, John Wiley.

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VII Semester

Biomedical Signal Processing			
Course Code	**21EC724**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

This course will enable students to:

- Possess the basic mathematical, scientific and computational skills necessary to analyse ECG and EEG signals.
- Apply classical and modern filtering and compression techniques for ECG and EEG signals.
- Develop a thorough understanding on basics of ECG and EEG feature extraction.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Biomedical Signals: The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives of Biomedical Signal analysis, Difficulties in Biomedical Signal analysis.
(Text-1: 1.1, 1.2, 1.3, 1.4)

Electrocardiography: Techniques used in electrocardiography, ECG Electrodes, the cardiac equivalent generator, genesis of the ECG, the standard and augmented limb leads, 12 lead ECG, the vectorcardiogram, ECG signal characteristics.
(Text-2: 2.1, 2.1.1, 2.1.2, 2.1.3, 2.1.4, 2.1.5, 2.2.1, 2.2.2, 2.3)

Signal Conversion: Simple signal conversion systems, Conversion requirements for biomedical signals, Signal converter characteristics, D to A converters, A to D converters, Sample and Hold circuit, Analog Multiplexer, Amplifiers
(Text-2: 3.2, 3.3, 3.4.1, 3.4.2, 3.4.3, 3.4.4, 3.4.5, 3.4.6).

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2, L3

Module-2

Signal Averaging: Basics of signal averaging, Signal averaging as a digital filter, a typical averager, Software for signal averaging, Limitations of signal averaging.
(Text-2: 9.1, 9.2, 9.3, 9.4, 9.5).

Adaptive Filters: Principal noise canceller model, 60-Hz adaptive cancelling using a sine wave model, Applications: Maternal ECG in fetal ECG, Cardiogenic artifact, detection of ventricular fibrillation and tachycardia. (Text-2: 8.1, 8.2, 8.3.1, 8.3.2, 8.3.3).

Teaching-Learning	Chalk and talk method, PowerPoint Presentation, YouTube videos

Process	**RBT Level:** L1, L2, L3
Module-3	
Data Reduction Techniques: Introduction, Turning point algorithm, AZTEC algorithm, Fano algorithm, Huffman coding: Static coding, Modified coding, Adaptive coding, Residual differencing, Runlength coding. (Text-2: 10.1, 10.2, 10.3, 10.4.1, 10.4.2, 10.4.3, 10.4.4, 10.4.5). **Time and Frequency domain techniques:** The Fourier transform for a discrete nonperiodic and periodic signals, the Fast Fourier transform, Correlation in time domain and in frequency domain, Convolution in time domain and in frequency domain, Power spectrum estimation: Parseval's theorem (Text-2: 11.1.1, 11.1.2, 11.1.3, 11.2.1, 11.2.2, 11.2.3, 11.3.1, 11.3.2, 11.3.3, 11.4.1)	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2, L3
Module-4	
ECG QRS detection: Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques: Template cross correlation, template subtraction, automata based template matching, a QRS detection algorithm. **ECG Analysis Systems:** Interpretation of the 12 lead ECG, ST segment analyzer, Portable arrhythmia monitor: Holter recording, software and hardware design, arrhythmia analysis (Text -2)	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2, L3
Module-5	
Neurological signal processing: The brain and its potentials, origin of brain waves, the EEG signal and its characteristics, EEG analysis, Linear prediction theory, The Autoregressive method, Recursive estimation of AR parameters, Spectral error measure. (Text-3: 4.1, 4.2, 4.3 4.4, 4.5, 4.6, 4.7, 4.8) **Event detection and waveform analysis:** EEG rhythms, waves and transients, Detection of EEG rhythms, Template matching for EEG spike and wave detection, the matched filter (Text-1: 4.2.4, 4.4.1, 4.4.2, 4.6)	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Describe the origin, properties and suitable models of important biological signals such as ECG and EEG.
2. Know the basic signal processing techniques in analysing biological signals.
3. Acquire mathematical and computational skills relevant to the field of biomedical signal processing.
4. Describe the basics of ECG signal compression algorithms.
5. Know the complexity of various biological phenomena.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester

3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Books:

1. Biomedical Signal Analysis-Rangaraj M Rangayyan, John Wiley & Sons 2002
2. Biomedical Digital Signal Processing- Willis J Tompkins, PHI2001.
3. Biomedical Signal Processing Principles and Techniques-D C Reddy, McGraw-Hill publications, 2005.

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VII Semester

Speech Signal Processing			
Course Code	**21EC725**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Introduce the models for speech production
- Develop Time domain and frequency domain speech processing techniques
- Introduce a predictive technique for speech compression
- Provide fundamental knowledge required to understand and analyze speech recognition, synthesis and speaker identification systems.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Fundamentals of Human Speech Production: The Process of Speech Production, Short-Time Fourier representation of Speech, The Acoustic Theory of Speech production, Digital Models for Sampled Speech Signals.

Teaching-Learning Process	Chalk and talk method, Power point presentations, Animation of process of speech production **RBT Level:** L1, L2, L3

Module-2

Time-Domain Methods for Speech Processing: Introduction to Short-Time Analysis of Speech, Short-Time Energy and Short-Time Magnitude, Short-Time Zero-Crossing Rate, The Short-Time Autocorrelation Function, Speech vs Silence detection.

Teaching-Learning Process	Chalk and talk method, Power point presentation Simulation of Short Time analysis algorithm using tools like Matlab/simulink **RBT Level:** L1, L2, L3

Module-3

Frequency Domain Representations: Discrete-Time Fourier Analysis, Short-Time Fourier Analysis, Overlap Addition (OLA) and Filter Bank Summation (FBS) Method of Synthesis, Time-Decimated Filter Banks, Two-Channel Filter Banks, Modifications of the STFT.

Teaching-Learning Process	Chalk and talk method, Power point presentation Visualization of speech using spectrogram **RBT Level:** L1, L2, L3

Module-4	
The Cepstrum and Homomorphic Speech Processing: Introduction, Homomorphic Systems for Convolution, Homomorphic Analysis of the Speech Model, Computing the Short-Time Cepstrum and Complex Cepstrum of Speech, Homomorphic Filtering of Natural Speech, Cepstrum Analysis of All-Pole Models, Cepstrum Distance Measures.	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Linear Predictive Analysis of Speech Signals: Introduction to Basic Principles of Linear Predictive Analysis, Computation of the Gain for the Model, Frequency Domain Interpretations of Linear Predictive Analysis, Solution of the LPC Equations, The Prediction Error Signal.	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Model speech production system and describe the fundamentals of speech.
2. Apply time domain and frequency domain algorithms, on speech to find, enhance and modify speech parameters.
3. Choose an appropriate processing technique for a given application.
4. Analyse speech recognition, synthesis and speaker identification systems

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question

papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books

1. **Digital Processing of Speech Signals** - L R Rabiner and R W Schafer, Pearson Education Asia, 2004.
2. **Theory and Applications of Digital Speech Processing**-Rabiner and Schafer, Pearson Education 2011.

Reference Books

1. **Fundamentals of Speech Recognition**- Lawrence Rabiner and Biing-Hwang Juang, Pearson Education, 2003.
2. **Speech and Language Processing**–An Introduction to Natural Language Processing, Computational Linguistics, and Speech Recognition- Daniel Jurafsky and James H Martin, Pearson Prentice Hall, 2009.

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VII Semester

IoT & Wireless Sensor Networks			
Course Code	**21EC731**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- To provide an exposure to the broad perspective of Internet of Things with respect to the characteristics, design, technologies and applications.
- To provide a basic understanding of the important aspects of Wireless sensor networks covering applications, sensor and transmission technology & systems, middleware, performance and traffic management.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the various concepts.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Internet of Things: Introduction, Physical design, Logical design, Enabling technologies, Levels & deployment templates.
Text 1: Chapter 1

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

Domain Specific IoTs: Home automation, cities, environment, energy, retail, logistics, agriculture, industry, health & lifestyle.
Text 1: Chapter 2

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3

Wireless Sensor Networks: Introduction, applications of sensor networks, basic overview of the technology, basic sensor network architectural elements, present day sensor network research, challenges and hurdles, examples of Category 2 WSN applications, examples of Category 1 WSN applications

Text 2: Chapter 1 – 1.1, 1.1.2, 1.2, 1.2.1, 1.2.2 (phase 4), 1.2.3 Chapter 2: 2.4, 2.5	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Wireless sensor technology: Introduction, sensor node technology – overview, hardware and software, sensor taxonomy, WN operating environment, WN trends. **Wireless Transmission technology and systems:** Introduction, Campus applications, MAN/WAN applications. Text 2: Chapter 3: 3.1, 3.2 – 3.2.1, 3.2.2, 3.3, 3.4, 3.5 Chapter 4: 4.1, 4.3.1, 4.3.2	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Middleware for WSNs: Introduction, principles, architecture, data related functions **Performance and traffic management:** background, WSN Design issues, performance modelling of WSNs. Text 2: Chapter 8: 8.1, 8.2, 8.3, 8.3.1 Chapter 11: 11.2, 11.3, 11.4	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the characteristics, building blocks, enabling technologies of the IoT systems
2. Describe the characteristics and applications of domain specific IoTs.
3. Discuss the overview of the Wireless sensor networks characteristics and applications.
4. Present the sensor, transmission technology and systems associated with WSN.
5. Understand the concepts of middleware, performance evaluation and traffic management in WSN.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per

the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. 'Internet of Things', Arshdeep Bagha and Vijay Madisetti, Universities Press, 2015
2. 'Wireless Sensor Networks', Kazem Sohraby, Daniel Minoli and Taieb Znati, Wiley, 2015.

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VII Semester

Network Security			
Course Code	**21EC732**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- **Preparation**: To prepare students with fundamental knowledge/ overview in the field of Network Security with knowledge of security mechanisms and services.
- **Core Competence**: To equip students with a basic foundation of Network Security by delivering the basics of Transport Level Security, Secure Socket Layer, Internet Protocol security, Intruders, Intrusion detection and Malicious Software, Firewalls, Firewall characteristics, Biasing and Configuration.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different Network Security Techniques / Algorithms
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes
10. Give Programming Assignments

Module-1

Attacks on Computers and Computer Security: Need for Security, Security Approaches, Principles of Security Types of Attacks. **(Text2: Chapter1)**
Security Mechanisms, Services and Attacks, A model for Network security **(Text1: Chapter1: 3, 4, 5, 6)**
Network Access Control, Extensible Authentication Protocol **(Text1: Chapter 16: Section 1,2)**

Teaching-Learning Process	Chalk and talk method, YouTube videos, Flipped Class Technique **RBT Level:** L1, L2, L3

Module-2

Transport Level Security: Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH) **(Text1: Chapter15)**

Teaching-Learning Process	Chalk and talk method YouTube videos, Flipped Class Technique and PPTs. Self-study topics: Block cipher modes, Cryptographic Hash functions and MAC codes **RBT Level:** L1, L2, L3

Module-3	
IP Security: Overview of IP Security (IPSec), IP Security Architecture, Modes of Operation, Security Associations (SA), Authentication Header (AH), Encapsulating Security Payload (ESP), Internet Key Exchange. **(Text1: Chapter19)**	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Flipped Class Technique and PPTs. Self-study topics: OSI Model **RBT Level:** L1, L2, L3
Module-4	
Intruders: Intruders, Intrusion Detection, Password Management. **(Chapter20-Text1)** **MALICIOUS SOFTWARE:** Viruses and Related Threats, Virus Countermeasures, **(Chapter21-Text1)**	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Flipped Class Technique and PPTs. **RBT Level:** L1, L2, L3
Module-5	
Firewalls: The Need for firewalls, Firewall Characteristics, Types of Firewalls, Firewall Biasing, Firewall location and configuration **(Chapter 22-Text 1)**	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Flipped Class Technique and PPTs. **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Explain network security services and mechanisms and explain security concepts
2. Understand the concept of Transport Level Security and Secure Socket Layer.
3. Explain Security concerns in Internet Protocol security
4. Explain Intruders, Intrusion detection and Malicious Software
5. Describe Firewalls, Firewall Characteristics, Biasing and Configuration

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per

the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 5th Edition, 2014, ISBN: 978-81-317- 6166-3
2. Atul Kahate, "Cryptography and Network Security", TMH, 2003.

Reference Books:

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.
2. Introduction to Computer Security, Matt Bishop, Sathyanarayana S V, Pearson Education, 2006, ISBN 81-7758-425/1.

Web links and Video Lectures (e-Resources)

https://nptel.ac.in/courses/106105031
https://nptel.ac.in/courses/128106006

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Programming Assignments / Mini Projects can be given to improve programming skills.

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VII Semester

Fabrication Technology			
Course Code	**21EC733**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Familiarise with the concepts of different processes involved in fabrication process and also with packaging issues.
- Apply principles to identify and analyse the various steps for the fabrication of various components.
- Introduce the fundamental concepts relevant to VLSI fabrication.
- Enable the students to understand the various VLSI fabrication techniques.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Topics will be introduced in multiple representations.
5. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Crystal Growth and Wafer Preparation: Introduction, Electronic grade Silicon, Czochralski Crystal Growing, Silicon Shaping

Epitaxy: Introduction, Vapor-Phase Epitaxy

Text Book 1.1 to 1.4, 2.1 to 2.2

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, Videos on crystal growth process Self-study topics: Mask Preparation **RBT Level:** L1, L2, L3

Module-2

Epitaxy: Molecular beam epitaxy, Epitaxial evaluation

Oxidation: Introduction, Growth mechanism and kinetics, Thin oxides, oxidation techniques, oxide properties, redistribution of dopants, oxidation of polysilicon, oxidation-induced defects

Text Book 2.3 and 2.5, 3.1 to 3.8

Teaching-Learning Process	Chalk and talk method, Power point presentation, videos on Epitaxial process Self-study topics: Advanced oxidation techniques **RBT Level:** L1, L2, L3

Module-3

Lithography: Introduction, Optical Lithography, Electron Lithography, X-ray lithography, Ion Lithography

Text Book 4.1 to 4.5

Teaching-	Chalk and talk method, PowerPoint Presentation, Videos on Lithography

Learning Process	Self-study topics: Sputtering and edge lithography **RBT Level:** L1, L2, L3

Module-4

Diffusion: Introduction, Models of diffusion in solids, fick's 1D diffusion equation, atomic diffusion mechanism, Diffussivities, Measurement techniques, fast diffusants in silicon, diffusion in polycrystalline silicon, diffusion in SiO2

Ion Implantation: Introduction, Implantation equipment

Text Book 7.1 to 7.9, 8.1 and 8.3

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, Videos on diffusion method Self-study topics: Effect of doping concentration in diffusion process **RBT Level:** L1, L2, L3

Module-5

Ion Implantation: Annealing, Shallow Junctions, High energy implantation

Metallization: Introduction, Metallization applications, metallization choices, Metallization problems, New role of metallization.

Text Book 8.4 to 8.6, 9.1 to 9.7 (except 9.4 and 9.5)

Teaching-Learning Process	Chalk and talk method, Power point presentation, Videos on Annealing process Self-study topics: e-beam evaporation, plasma spray deposition **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Understanding the process in the field of Fabrication technology.
2. Understand the properties and growth mechanism of oxidation.
3. Relate to the competing methods of various lithographic techniques and their limitations.
4. Analyse the diffusion profiles and models in various materials.
5. Describe the Metallization choices, properties and selection of optimum deposition process.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per

the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Book:

VLSI Technology, S M Sze, 2nd edition, Mc Graw Hill.

Reference Books:

1. VLSI Fabrication Principles, S K Gandhi, John Willey & Sons.
2. Micromachined transducer, G T A Kovacs, McGraw Hill.

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VII Semester

Machine Learning with Python			
Course Code	**21EC734**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:0: 2:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- To understand the basic theory underlying machine learning.
- To be able to formulate machine learning problems corresponding to different applications.
- To understand a range of machine learning algorithms along with their strengths and weaknesses.
- To be able to apply machine learning algorithms to solve problems of moderate complexity.
- To apply the algorithms to a real-world problem, optimize the models learned and report on the expected accuracy that can be achieved by applying the models.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop student's theoretical and programming skills.
2. State the need for learning Machine Learning with real-life examples.
3. Support and guide the students for self–study.
4. You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students & progress
5. Encourage the students for group learning to improve their creative and analytical skills.
6. Show short, related video lectures in the following ways:
    - As an introduction to new topics (pre-lecture activity).
    - As a revision of topics (post-lecture activity).
    - As additional examples (post-lecture activity).
    - As an additional material of challenging topics (pre-and post-lecture activity).
    - As a model solution of some real world problems. (post-lecture activity).

Module-1

Introduction:

Introduction to Machine Learning, Building intelligent machines to transform data into knowledge, The three different types of machine learning, An introduction to the basic terminology and notations, A roadmap for building machine learning systems, Using Python for machine learning.

Training Machine Learning Algorithms for Classification

Artificial neurons – a brief glimpse into the early history of machine learning, Implementing a perceptron learning algorithm in Python, Adaptive linear neurons and the convergence of learning.

Textbook 1: Chapters 1, 2

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

A Tour of Machine Learning Classifiers Using Scikit-Learn

Choosing a classification algorithm, First steps with scikit-learn, Modeling class probabilities via logistic regression, Maximum margin classification with support vector machines, Solving nonlinear problems using a kernel SVM, Decision tree learning, K-nearest neighbors – a lazy learning algorithm

Building Good Training Sets – Data Preprocessing Dealing with missing data, Handling categorical data, Partitioning a dataset in training and test sets, Bringing features onto the same scale, Selecting meaningful features, Assessing feature importance with random forests. Textbook 1: Chapters 3 ,4	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-3	
Compressing Data via Dimensionality Reduction Unsupervised dimensionality reduction via principal component Analysis, Supervised data compression via linear discriminant analysis, Using kernel principal component analysis for nonlinear mappings **Learning Best Practices for Model Evaluation and Hyperparameter Tuning** Streamlining workflows with pipelines, Using k-fold cross-validation to assess model performance, Debugging algorithms with learning and validation curves, Fine-tuning machine learning models via grid search, Looking at different performance evaluation metrics **Applying Machine Learning to Sentiment Analysis** Obtaining the IMDb movie review dataset, Introducing the bag-of-words model, training a logistic regression model for document classification , Working with bigger data – online algorithms and out-of-core learning Textbook 1: Chapters 5,6,8	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Embedding a Machine Learning Model into a Web Application Serializing fitted scikit-learn estimators, Setting up a SQLite database for data storage, Developing a web application with Flask, Turning the movie classifier into a web application, Deploying the web application to a public server **Predicting Continuous Target Variables with Regression Analysis** Introducing a simple linear regression model, Exploring the Housing Dataset, Implementing an ordinary least squares linear regression model, Fitting a robust regression model using RANSAC, Evaluating the performance of linear regression models, Using regularized methods for regression- Turning a linear regression model into a curve – polynomial regression Textbook 1: Chapters 9,10	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Working with Unlabeled Data – Clustering Analysis Grouping objects by similarity using k-means, Organizing clusters as a hierarchical tree, **Training Artificial Neural Networks for Image Recognition** Modeling complex functions with artificial neural networks, Classifying handwritten digits, Training an artificial neural network, Other neural network architectures Textbook 1: Chapters 11,12	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Appreciate the importance of visualization in the data analytics solution
2. Apply structured thinking to unstructured problems
3. Understand a very broad collection of machine learning algorithms and problems
4. Learn algorithmic topics of machine learning and mathematically deep enough to introduce the required theory
5. Develop an appreciation for what is involved in learning from data.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Python Machine Learning by Sebastian Raschka, Published by Packt Publishing Ltd.
2. Machine Learning with Python for Everyone by Mark E Fenner
3. Machine Learning using Python by Manaranjan Pradhan & U Dinesh Kumar
4. Practical Machine Learning with Python by Dipanjan Sarkar, Raghav Bali &Tushar Sharma

Web links and Video Lectures (e-Resources)
• https://www.youtube.com/watch?v=RnFGwxJwx-0 • https://www.youtube.com/watch?v=eq7KF7JTinU
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Using IRIS data set implement Adaline rule Classification Algorithm. • Implement Logistic Regression algorithm and generate corresponding graphs for overfitting and under fitting. • Implement linear SVM algorithm with maximum margin intuition. • Implement a kernel SVM to solve nonlinear problems. • Implement KNN Algorithm. • Implement decision tree algorithm. • Implement s rbf_kernel_pca for separating half-moon shapes. • Develop web application using flask.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

VII Semester

Multimedia Communication			
Course Code	**21EC735**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

This course will enable students to:

- Understand the importance of multimedia in today's online and offline information sources and repositories.
- Understand the how Text, Audio, Image and Video information can be represented digitally in a computer so that it can be processed, transmitted and stored efficiently.
- Understand the Multimedia Transport in Wireless Networks
- Understand the Real-time multimedia network applications.
- Understand the Different network layer based application.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Topics will be introduced in multiple representations.
6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1	
Multimedia Communications: Introduction, Multimedia information representation, Multimedia networks, multimedia applications, Application and networking terminology. (Chapter 1 of Text 1)	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2
Module-2	
Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video. (Chapter 2 of Text 1)	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-3	
Text and Image Compression: Introduction, Compression principles, text compression, image Compression. (Chapter 3 of Text 1)	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-4	
Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression. (Chapter 4 of Text 1)	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI High-speed LANs, LAN protocol (Chap. 8 of Text 1).	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand basics of different multimedia networks and applications.
2. Understand different compression techniques to compress audio and video.
3. Describe multimedia Communication across Networks.
4. Analyse different media types to represent them in digital form.
5. Compress different types of text and images using different compression techniques.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored

out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

Multimedia Communications- Fred Halsall, Pearson Education, 2001, ISBN -978813170994

Reference Books:

1. Multimedia: Computing, Communications and Applications- Raif Steinmetz, Klara Nahrstedt, Pearson Education, 2002, ISBN-978817758
2. Fundamentals of Multimedia – Ze-Nian Li, Mark S Drew, and Jiangchuan Liu.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Implementation of compression algorithms using MATLAB/ any open source tools (Python, Scilab, etc.)

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III SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	/	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21MAT31	Transform Calculus, Fourier Series And Numerical Techniques	Maths	2	2	0	0	03	50	50	100	3
2	IPCC 21ME32	Metal casting, Forming and Joining Processes	TD: ME PSB: ME	3	0	2	0	03	50	50	100	4
3	IPCC 21ME33	Material Science and Engineering	TD: ME PSB ME	3	0	2	0	03	50	50	100	4
4	PCC 21ME34	Thermodynamics	TD: ME PSB ME	2	2	0	0	03	50	50	100	3
5	PCC 21MEL35	Machine Drawing and GD & T	TD: ME PSB ME	0	0	2	0	03	50	50	100	1
6	UHV 21UH36	Social Connect and Responsibility	Any Department	0	0	1	0	01	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	TD and PSB: HSMC	1	0	0	0	01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India and Professional Ethics										
8	AEC 21ME38X	Ability Enhancement Course – III	TD: Concerned department PSB: Concerned Board	If offered as Theory Course				01	50	50	100	1
				0	2	0						
				If offered as lab. course				02				
				0	0	2						
								Total	**400**	**400**	**800**	**18**

9	**Scheduled activities for III to VIII semesters**	NMDC 21NS83	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester.The activities shall be carried out from (for 5 semesters) between III semester to VIII semester. SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the colander prepared for
		NMDC 21PE83	Physical Education (PE)(Sports and Athletics)	PE	
		NMDC 21YO83	Yoga	Yoga	

					the NSS, PE and Yoga activities.							
Course prescribed to lateral entry Diploma holders admitted to III semester B.E./B.Tech programs												
1	NCMC 21MATDIP31	Additional Mathematics - I	Maths	02	02	--	--	---	100	---	100	0

Note:BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course,**INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course.

L –Lecture, **T –** Tutorial, P- Practical/ Drawing, **S –** Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD-** Teaching Department, **PSB**: Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and **21KBK37/47** Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practicals of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

21INT49 Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internshipof 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card.The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A)Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and has no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the coursesAdditional Mathematics I and IIshall be indicated as satisfactory in the grade card. Non-completion of the courses. Additional Mathematics I and IIshall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they has to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Ability Enhancement Course – III			
21ME381	Introduction to PYTHON (0-0-2-0)	21ME383	Digital Society(0-2-0-0)
21ME382	Fundamentals of Virtual Reality (0-2-0-0)		

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IV SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical / Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21ME41	Complex Analysis, Probability and Linear Programming.	Maths	2	2	0	0	03	50	50	100	3
2	IPCC 21ME42	Machining Science and Jigs & Fixtures	TD: ME PSB: ME	3	0	2	0	03	50	50	100	4
3	IPCC 21ME43	Fluid Mechanics	TD: ME PSB: ME	3	0	2	0	03	50	50	100	4
4	PCC 21ME44	Mechanics of Materials	TD: ME PSB: ME	2	2	0	0	03	50	50	100	3
5	AEC 21BE45	Biology For Engineers	BT, CHE, PHY	2	0	0	0	02	50	50	100	2
6	PCC 21MEL46	Mechanical Measurements and Metrology Lab	TD: ME PSB: ME	0	0	2	0	03	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	HSMC	1	0	0	0	01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India & Professional Ethics										
8	AEC 21XX48X	Ability Enhancement Course- IV	TD and PSB: Concerned department	If offered as theory Course: 0	2	0		01	50	50	100	1
				If offered as lab. Course: 0	0	2		02				
9	UHV 21UH49	UniversalHumanValues	Any Department	1	0	0		01	50	50	100	1
10	INT 21INT49	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period ofII and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.				3	100	--	100	2

								Total	**550**	**450**	**1000**	**22**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs												
1	NCMC 21MATDIP41	Additional Mathematics – II	Maths	02	02	--	--	--	100	--	100	0

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L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

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Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practicals of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from practical part of IPCCshall be included in the SEE question paper.For more details the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

Non – credit mandatory course (NCMC):

Additional Mathematics - II:

(1) Lateral entry Diploma holders admitted to III semester of B.E./B.Tech., shall attend the classes during the IV semester to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and has no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the course Additional Mathematics IIshall be indicated as satisfactory in the grade card. Non-completion of the coursesAdditional Mathematics IIshall be indicated as Unsatisfactory.

Ability Enhancement Course – IV			
21ME481	Spread Sheets for Engineers (0-0-2-0)	21ME483	Fundamentals of Augmented Reality (0-2-0-0)
21ME482	Introduction to AI and ML (0-2-0-0)		

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68Innovation/ Entrepreneurship/ Societalbased Internship.

(1) All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card.The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be considered under F (fail) grade and shall have to complete during subsequently after satisfying the internship requirements.

(2) Innovation/ Entrepreneurship Internshipshall be carried out at industry, State and Central Government /Non-government organizations (NGOs), micro, small and medium enterprise (MSME), Innovation centers or Incubation centers. Innovation need not be a single major breakthrough, it can also be a series of small or incremental changes.Innovation of any kind can also happen outside of the business world.

Entrepreneurship internships offers a chance to gain hands on experience in the world of entrepreneurship and helps to learn what it takes to run a small entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business endeavours.Start-ups and small companies are a preferred place to learn the business tack ticks for future entrepreneurs as learning how a small business operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open the minds to creativity and innovation.Entrepreneurship internship can be from several sectors, including technology, small and medium-sized, and the service sector.

(3) Societal or social internship.

Urbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of

many things that urban population enjoy. Rural internship, is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for better living. As proposed under the AICTE rural internship programme, activities under Societal or social internship, particularly in rural areas, shall be considered for 40 points under AICTE activity point programme.

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V SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	/	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21ME51	Theory of Machines	TD: ME PSB: ME	2	2	0	0	03	50	50	100	3
2	IPCC 21ME52	Thermo-fluids Engineering	TD: ME PSB: ME	3	0	2	0	03	50	50	100	4
3	PCC 21ME53	Finite Element Analysis	TD: ME PSB: ME	2	0	2	0	03	50	50	100	3
4	PCC 21ME54	Modern Mobility and Automotive Mechanics	TD: ME PSB: ME	3	0	0	0	03	50	50	100	3
5	PCC 21MEL55	Design lab	TD: ME PSB: ME	0	0	2	0	03	50	50	100	1
6	AEC 21XX56	Research Methodology & Intellectual Property Rights	TD: Any Department PSB: As identified by University	2	0	0	0	02	50	50	100	2
7	HSMC 21CIV57	Environmental Studies	TD: Civil/ Environmental /Chemistry/ Biotech. PSB: Civil Engg	2	0	0	0	1	50	50	100	1
8	AEC 21ME58X	Ability Enhancement Course-V	Concerned Board	If offered as Theory courses: 0	2	0		01	50	50	100	1
				If offered as lab.Courses: 0	0	2		02				
								Total	**400**	**400**	**800**	**18**

Ability Enhancement Course – IV

21ME581	Basics of MATLAB(0-0-2-0)	21ME583	VFX – Visual Effects (0-2-0-0)
21ME582	Digital Marketing (0-2-0-0)		

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L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Integrated Professional Core Course (IPCC): refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). Theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by CIE only and there shall be no SEE. For more details the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech.) 2021-22 may be referred.

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VI SEMESTER

Sl. No	Course and Course Code	Course Title	Department (TD) and Question Paper Setting Board	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	/	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	HSMC 21ME61	Production and Operations Management	TD: ME PSB: ME	3	0	0	0	03	50	50	100	3
2	IPCC 21ME62	Heat Transfer	TD: ME PSB: ME	3	0	2	0	03	50	50	100	4
3	PCC 21ME63	Machine design	TD: ME PSB: ME	2	2	0	0	03	50	50	100	3
4	PEC 21ME64x	ProfessionalElective Course-I	TD: ME PSB: ME	3	0	0	0	03	50	50	100	3
5	OEC 21ME65x	OpenElective Course-I	TD: ME PSB: ME	3	0	0	0	03	50	50	100	3
6	PCC 21MEL66	CNC Programming and 3-D Printing Lab	TD: ME PSB: ME	0	0	2	0	03	50	50	100	1
7	MP 21MEMP67	Mini Project		Two contact hours /week for interaction between the faculty and students.				--	100	--	100	2
8	INT 21INT68	Innovation/Entrepreneurship /Societal Internship	Completed during the intervening period of IV and V semesters.					--	100	--	100	3
								Total	**500**	**300**	**800**	**22**

Professional Elective – I			
21ME641	Supply Chain Management & Introduction to SAP	21ME643	Autonomous vehicles
21ME642	Mechatronic System Design	21ME644	Internet of Things (IoT) (2-0-2-0)

Open Electives – I offered by the Department to other Department students			
21ME651	Project Management	21ME653	Mechatronics
21ME652	Renewable Energy Power Plants	21ME654	Modern Mobility

Note: HSMC: Humanity and Social Science & Management Courses, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **PEC:** Professional Elective Courses, O**EC**–Open Elective Course, **MP** –Mini Project, INT – Internship.

L –Lecture, T – Tutorial, P - Practical / Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with Practical of the same course. Credit for IPCC can be 04 and its Teaching – Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by CIE only and there shall be no SEE. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (BE/B.Tech) 2021-22 may be referred.

Professional Elective Courses(PEC):

A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the

Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course out of five course. The minimum students' strength for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the programme is less than 10.

Open Elective Courses:

Students belonging to a particular stream of Engineering and Technology are not entitled for the open electives offered by their parent Department. However, they can opt an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor.

Selection of an open elective shall **not be allowed** if,

(i) The candidate has studied the same course during the previous semesters of the program.

(ii) The syllabus content of open electives is similar to that of the Departmental core courses or professional electives.

(iii) A similar course, under any category, is prescribed in the higher semesters of the program.

In case, any college is desirous of offering a course (not included in the Open Elective List of the University) from streams such as Law, Business (MBA), Medicine, Arts, Commerce, etc., can seek permission, at least one month before the commencement of the semester, from the University by submitting a copy of the syllabus along with the details of expertise available to teach the same in the college.

The minimum students' strength for offering open electives is 10. However, this conditional shall not be applicable to cases where the admission to the programme is less than 10.

Mini-project work: Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications.

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.

CIE procedure for Mini-project:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two faculty members of the Department, one of them being the Guide. The CIE marks awarded for the Mini-project work shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the project.

The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

No SEE component for Mini-Project.

VII semester Classwork and Research Internship /Industry Internship (21INT82)

Swapping Facility

Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate research internship/ industry internship after the VI semester**.**

(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the program.

Elucidation:

At the beginning of IV year of the programme i.e., after VI semester, VII semester classwork and VIII semester Research Internship /Industrial Internship shall be permitted to be operated simultaneously by the University so that students have ample opportunity for internship. In other words, a good percentage of the class shall attend VII semester classwork and similar percentage of others shall attend to Research Internship or Industrial Internship.

Research/Industrial Internship shall be carried out at an Industry, NGO, MSME, Innovation centre, Incubation centre, Start-up, Centers of Excellence (CoE), Study Centre established in the parent institute and /or at reputed research organizations / institutes. The intership can also be rural internship.

The mandatory Research internship /Industry internship is for 24 weeks. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during the subsequent University examination after satisfying the internship

requirements.

INT21INT82 Research Internship/ Industry Internship/Rural Internship

Research internship: A research internship is intended to offer the flavour of current research going on in the research field. It helps students get familiarized with the field and imparts the skill required for carrying out research.

Industry internship: Is an extended period of work experience undertaken by students to supplement their degree for professional development. It also helps them learn to overcome unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with contingencies helps students recognize, appreciate, and adapt to organizational realities by tempering their knowledge with practical constraints.

Rural internship: A long-term goal, as proposed under the AICTE rural internship programme, shall be counted as rural internship activity.

The student can take up Interdisciplinary Research Internship or Industry Internship.

The faculty coordinator or mentor has to monitor the students' internship progress and interact with them to guide for the successful completion of the internship.

The students are permitted to carry out the internship anywhere in India or abroad. University shall not bear any expenses incurred in respect of internship.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E. in MECHANICAL ENGINEERING
Scheme of Teaching and Examinations 2021
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 - 22)

Swappable VII and VIII SEMESTER

VII SEMESTER

Sl. No	Course and Course Code	Course Title	Department (TD) and Question Paper Setting Board	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical / Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	PCC 21ME71	Automation and Robotics	TD: ME PSB: ME	3	0	0	0	3	50	50	100	3
2	PCC 21ME72	Control Engg	TD: ME PSB: ME	3	0	0	0	3	50	50	100	2
3	PEC 21ME73X	Professional elective Course-II	TD: ME PSB: ME	3	0	0	0	3	50	50	100	3
4	PEC 21ME74X	Professional elective Course-III	TD: ME PSB: ME	3	0	0	0	3	50	50	100	3
5	OEC 21ME75X	Open elective Course-II	TD: ME PSB: ME	3	0	0	0	3	50	50	100	3
6	Project 21MEP76	Project work		Two contact hours /week for interaction between the faculty and students.				3	100	100	200	10
								Total	**350**	**350**	**700**	**24**

VIII SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical / Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	Seminar 21XX81		Technical Seminar		One contact hour /week for interaction between the faculty and students.				--	100	--	100	01
2	INT 21INT82		Research Internship/ Industry Internship		Two contact hours /week for interaction between the faculty and students.				03 (Batch wise)	100	100	200	15
3	NCMC	21NS83	National Service Scheme (NSS)	NSS	Completed during the intervening period of III semester to VIII semester.				--	50	50	100	0
		21PE83	Physical Education (PE) (Sports and Athletics)	PE									
		21YO83	Yoga	Yoga									
									Total	**250**	**150**	**400**	**16**

Professional Elective – II

21ME731	Additive Manufacturing	21ME734	MEMS and Microsystem Technology
21ME732	Total Quality Management	21ME735	Design for Manufacturing and Assembly
21ME733	Refrigeration and Air conditioning		
Professional Elective – III			
21ME741	Advanced Vibrations and Condition Monitoring	21ME744	Product Design and Ergonomics
21ME742	Theory and Design of IC Engines		
21ME743	Advanced Turbomachines		

Open Electives - II offered by the Department to other Department students			
21ME751	Non-traditional Machining	21ME7533	Operations Research
21ME752	Hydraulics and Pneumatics		

Note: PCC: Professional Core Course, **PEC:** Professional Elective Courses, **OEC**–Open Elective Course, **AEC** –Ability Enhancement Courses.

L –Lecture, T – Tutorial, P- Practical / Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Note: VII and VIII semesters of IV year of the programme

(1) Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate research internship/ industry internship after the VI semester**.**

(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against

PROJECT WORK (21XXP75): The objective of the Project work is

(i) To encourage independent learning and the innovative attitude of the students.

(ii) To develop interactive attitude, communication skills, organization, time management, and presentation skills.

(iii) To impart flexibility and adaptability.

(iv) To inspire team working.

(v) To expand intellectual capacity, credibility, judgment and intuition.

(vi) To adhere to punctuality, setting and meeting deadlines.

(vii) To instill responsibilities to oneself and others.

(viii) To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

CIE procedure for Project Work:

(1) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(2) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all

TECHNICAL SEMINAR (21XXS81): The objective of the seminar is to inculcate self-learning, present the seminar topic confidently, enhance communication skill, involve in group discussion for exchange of ideas. Each student, under the guidance of a Faculty, shall choose, preferably, a recent topic of his/her interest relevant to the programme of Specialization.

(i) Carry out literature survey, systematically organize the content.

(ii) Prepare the report with own sentences, avoiding a cut and paste act.

(iii) Type the matter to acquaint with the use of Micro-soft equation and drawing tools or any such facilities.

(iv) Present the seminar topic orally and/or through PowerPoint slides.

(v) Answer the queries and involve in debate/discussion.

(**vi)** Submit a typed report with a list of references.

The participants shall take part in the discussion to foster a friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Evaluation Procedure:

The CIE marks for the seminar shall be awarded (based on the relevance of the topic, presentation skill, participation in the question and answer session, and quality of report) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three teachers from the department with the senior-most acting as the Chairman.

Marks distribution for CIE of the course:

Seminar Report:50 marks

Presentation skill:25 marks

Question and Answer: 25 marks. ■ No SEE component for Technical Seminar

Non – credit mandatory courses (NCMC):

National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they has to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequently to earn the qualifying CIE marks subject to the maximum programme period.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These course shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Vivekananda College of Engineering & Technology, Puttur, D.K 574 203

(A UNIT of VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR ®)

RECEIPTS AND PAYMENTS ACCOUNTS FOR THE YEAR ENDING 31st MARCH 2020

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
To **Tuition and Other Fees**			**By Staff Salary and Allowances**		
a) **Tuition fee**		7,16,49,454.00	Salary of Teaching Staff	6,10,00,917.00	
b) **Specific fees:**			Non-Teaching Staff	1,15,95,317.00	
Annual College Fees	2,96,24,157.00		Menial Staff	7,89,649.00	
Book Bank	17,66,500.00		Gratuity	4,23,104.00	7,38,08,987.00
Dept. Asso. Fee	5,45,000.00				
Graduation Day	3,23,250.00		**By Specific Expenses:**	6,75,000.00	
IOT Lab Fee	12,09,930.00		Book Bank	2,70,016.00	
Jnana Sangama	1,26,000.00		Co-curricular activities/Association	9,14,925.00	
Lesson Plan	5,95,200.00		College Day	6,21,152.00	
Record Book	1,58,800.00		College Internal Examinations	6,530.00	
Training Fee	29,70,300.00	3,73,19,137.00	Graduation Day Exps	3,36,289.00	
			IOT Lab Exp's	1,08,340.00	
c) **Miscellaneous Fees:**			Jnana Sangama	98,687.00	
Karnataka State Student Welfare Fund	34,750.00		Library Books	49,541.00	
Karnataka State Teachers Benefit Fund	34,750.00		Reading Room	92,382.00	
National Foundation For Teachers Welfare	34,750.00		Sports Equipments/expenses	6,02,398.00	
NSS Fee	54,600.00		Student Welfare	1,04,673.00	
Red Cross	69,415.00		SCIENTIA	93,192.00	
Vidya Bharathi	22,650.00		NCASEM 2019	1,50,640.00	41,23,765.00
Vidya Nidhi	2,72,600.00	5,23,515.00			
d) **Universtiy Fees**			By **Other Miscellaneous Payments - University Fees**		
Change of Branch	30,000.00		Change of Branch	30,000.00	
Convocation Fees	4,06,400.00		Convocation Fees	4,06,400.00	
E-Learning fees	6,45,400.00		E-Learning fees	6,46,000.00	
Eligibility certificate fee	3,49,500.00		Eligibility certificate fee	3,73,000.00	
Exit Scheme Fee	.00		Exit Scheme Fee	28,000.00	
Revaluation fees	4,38,355.00		Revaluation fees	3,19,200.00	
Univ.Exam. Remuneration A/c	11,25,390.00		Univ.Exam. Remuneration A/c	9,32,668.00	
University Examination fee	41,43,195.00		University Examination fee	42,11,645.00	
University Fees	12,47,605.00		University Fees	9,62,730.00	
VTU Consortium Fee	10,99,500.00		VTU Consortium Fee	11,56,250.00	
C/F	**94,85,345.00**	**10,94,92,106.00**	**C/F**	**90,65,893.00**	**7,79,32,752.00**

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
B/F	94,85,345.00	10,94,92,106.00	B/F	90,65,893.00	7,79,32,752.00
VTU Exam Application	54,640.00		VTU Registration Fee	5,91,675.00	
VTU Registration Fee	5,30,624.00	1,00,70,609.00	VTU Exam Application	31,350.00	96,88,918.00
To Miscellaneous Receipts					
Admission Process Fee	1,64,000.00		By **Miscellaneous Fees: - Remittances**		
Consultancy Civil	5,08,477.00		Karnataka State Student Welfare Fund	13,995.00	
Consultancy Mech	.00		Karnataka State Teachers Benefit Fund	34,800.00	
Fine & Miscellaneous Receipts	3,60,662.00		National Foundation For Teachers Welfare	38,680.00	
Intrest on Bank Accounts	3,98,448.00		NSS Fee	.00	
Lab Breakages	1,88,940.00		Red Cross	21,060.00	
Online Test Lab Charges	70,980.00		Vidya Bharathi	20,880.00	
Processing Charges	1,11,500.00		Vidya Nidhi	2,78,400.00	4,07,815.00
RV / Photo Copy Appl. Fee	12,320.00	18,15,327.00			
			By Contingencies:		
To Scholarships			Advertisment / Publicity	1,64,508.00	
Fee Concession OBC Students	1,29,55,000.00		Affiliation/Inspection fees	4,36,000.00	
Fee Concession SC/ST Students	30,32,360.00		Bank Commission	21,985.54	
Arivu Loan (Minority Dept.)	22,58,801.00	1,82,46,161.00	Building Maintenance	5,36,336.00	
			Electrical Fittings and Wiring	7,75,110.00	
To Salary Deductions			Fright & Carriage	13,850.00	
Employees Provident Fund	33,02,543.00		Institute Image Building (IIBC)	2,67,497.00	
ESI	1,03,518.00		Internet Leased Line	12,14,053.00	
Labour Welfare Fund	3,460.00		Miscellaneous Expenses	30,163.00	
Life Insurance Premium	14,37,213.00		Office Automation Software	.00	
Profession Tax	3,05,000.00		Photo Copier Expenses	1,42,290.00	
TDS	18,73,980.00	70,25,714.00	Placement/Training	12,92,783.00	
			Postage, Telegram & Telephone	1,02,771.00	
To Grants			Printing & Stationery	4,01,100.00	
Grant KSCST	47,500.00		Professional charges	1,090.00	
Grant - VTU	2,81,345.00		RV / Photo Copy Appl. Fee	3,650.00	
Grant - NSS	.00		Staff Welfare	28,424.00	
Grant - Other	11,000.00		Travelling expenses	1,73,705.20	
Grant - NAIN	.00		Travelling expenses -Directors	401.00	
Grant - EDII (GOVT.)	20,000.00		Workshop/Seminar	1,09,166.00	57,14,882.74
C/F	3,59,845.00	14,66,49,917.00	C/F		9,37,44,367.74

RECEIPTS		Amount (Rs.)		PAYMENTS		Amount (Rs.)	
	B/F	3,59,845.00	14,66,49,917.00		B/F		9,37,44,367.74
Grant - VGST		7,33,390.00	10,93,235.00	**By Consumables:**			
				Chemistry		61,564.00	
To Advace and Refund (as per schdule)			28,59,331.00	Civil		30,712.00	
To TDS - Others			1,24,083.00	Computer Science		4,441.00	
TO TDS on Bills Receivable				Electronics		34,344.00	
To Unnath Bharath Abhiyan			.00	IT Cell		57,042.00	
To VTU E-shikshana			.00	Library		.00	
To ISTE Membership Fee			.00	Mechanical		47,652.00	
To ID Card			4,700.00	Physics		1,746.00	2,37,501.00
To Caution Deposit			87,250.00	By **Repairs and Maintance**			
TO NSS ACTIVITY			.00	General Repairs and Maintenance		1,01,613.00	
To NCASEM 2019			2,57,800.00	Generator Maintenance		6,79,081.00	
To R&D MECHANICAL (PRIZE)			10,000.00	Maintenance of Premises		5,89,721.00	
				Maintenance of Vehicle		1,11,936.00	
				Repairs to Chem Lab equipmt.		2,056.00	
				Repairs to CS Lab equipmt.		82,911.00	
				Repairs to CV Lab equipmt.		31,653.00	
To NAIN INT. ON BANK A/C			10,428.00	Repairs to E & C Lab equipmt.		10,726.00	
				Repairs to IT Cell		3,31,383.00	
				Repairs to mba Lab equipmt.		3,953.00	
				Repairs to Mech. Lab equipmt.		77,052.00	20,22,085.00
				By **Scholarships**			
				Fee Concession OBC Students		1,20,94,950.00	
				Fee Concession SC/ST Students		30,69,980.00	
				Arivu Loan (Minority Dept.)		20,57,260.00	
				Scholarship other		2,27,906.00	1,74,50,096.00
				By **Laboratory Equipments:**			
				CCP LAB		3,81,000.00	
				Chemistry		5,286.00	
				Civil		98,383.00	
				CS		2,22,511.00	
				EC		2,15,857.00	
				IT Infrastructure		6,49,578.00	
				Mechanical		3,57,382.00	
				Physics		2,100.00	19,32,097.00
				By Adv. & Refund			4,73,324.00
	C/F		15,10,96,744.00		C/F		11,58,59,470.74

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
B/F	.00	15,10,96,744.00	B/F		11,58,59,470.74
			By Alumni		72,974.00
			By Consultancy Civil		.00
			By Consultancy Mech		.00
			By Furniture and Fixtures		10,64,570.00
			By Office Equipment		69,950.00
			By TDS - Other		1,01,320.00
			By TDS on Bills Receivable		1,12,549.60
			By CII MEMBERSHIP FEE		5,605.00
			By DEPT INFRASTRUCTURE		4,33,156.00
			By **Salary Deductions**		
			Employees Provident Fund	33,02,543.00	
			ESI	1,03,518.00	
			Labour Welfare Fund	3,460.00	
			Life Insurance Premium	13,16,785.00	
			Profession Tax	3,05,000.00	
			TDS	18,73,980.00	69,05,286.00
			By **Transferred to:**		
			Vivekananada Vidyavardhaka Sangha Puttur ®		2,30,49,638.10
			By **Grants**		
			Grant - ISTE	7,500.00	
			Grant - Other	11,000.00	
			Grant KSCST	58,000.00	
			Grant- VGST	20,40,297.60	
			Grant- VTU	6,050.00	
			Grant - EDII (GOVT.)	31,000.00	
			NSS Activity	3,460.00	21,57,307.60
			By Unnath Bharath Abhiyan		48,223.00
			By ADMINISTATIVE OVERHEAD		67,300.00
			By Software		4,31,936.00
			By ISTE Membership Fee (Remittance)		27,405.00
			By VTU E-shikshana		3,600.00
			By Meeting & Function Exps		40,245.00
			By CCTV SECURITY SYSTEMS		11,90,940.00
			By ID Card		38,761.00
C/F		15,10,96,744.00	C/F		15,16,80,237.04

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
B/F	.00	15,10,96,744.00	B/F		15,16,80,237.04
			BY KEA FEES		3,500.00
			By KSCST STUDENT PROJECT		8,000.00
			By RED CROSS EXP'S		8,220.00
			By R&D MECHANICAL		39,684.00
			By R&D E & C		35,933.00
			By TECH SAMVRT 2019		56,510.00
			By VIJNANA VIBHA		4,78,806.00
			By VIVEKA SANKALPA		3,990.00
			By E-TENDERING EXPENSES		21,000.00
			By NAIN OPEX FUND		
			NAIN - SALARY		3,24,500.00
			NAIN EVENTS		78,663.00
			NAIN MENTOR EXPENDITURE		7,500.00
			NAIN Meeting Exp's		12,765.00
			NAIN ADVT / PUBLICITY		2,835.00
			NAIN BANK COMMN.		234.00
To Opening Balance			By **Closing Balance**		
Cash in Hand	15,720.60		Cash in Hand		13,757.60
Cash at Bank			**Cash at Bank**		
Axis Bank	40,602.98		Axis Bank		.00
State Bank of India	1,06,908.00		State Bank of India		85,933.00
Canara Bank S.B.A/c No.72675	18,115.81		Canara Bank S.B.A/c No.72675		.00
Canara Bank S.B.A/c No.64	74,006.14		Canara Bank S.B.A/c No.64		34,953.16
Canara Bank S.B.A/c No.66	50,675.25		Canara Bank S.B.A/c No.66		3,21,184.58
Canara Bank S.B.A/c No.742	49,746.00		Canara Bank S.B.A/c No.742		51,473.00
Canara Bank S.B.A/c No.784	7,14,825.00		Canara Bank S.B.A/c No.784		12,10,028.00
Canara Bank S.B.A/c No.1088	2,02,436.25		Canara Bank S.B.A/c No.1088		2,69,091.25
Canara Bank S.B.A/c No.6355	1,013.00		Canara Bank S.B.A/c No.6355		1,049.00
Canara Bank S.B.A/c No.6357	4,70,136.00		Canara Bank S.B.A/c No.6357		44,607.00
Canara Bank S.B.A/c No.6401	19,86,523.00	37,30,708.03	Canara Bank S.B.A/c No.6401		32,998.40
		15,48,27,452.03			**15,48,27,452.03**

CORRESPONDENT TREASURER PRINCIPAL

AUDITOR'S CERTIFICATE

I certify that I have audited the Accounts of Vivekananda College of Engineering & Technology for the year ending on 31-03-2020 and that the Receipts and Payments shown in the above statement are correctly stated and supported by proper vouchers.

Place:Puttur
Date: 16-10-2020

S. RAMA BHAT, B.Com., F.C.A.
A.P.M.C. Road
PUTTUR - 574 201
Mem. No. 012673
Chartered Accountant

S. Rama Bhat

S. RAMA BHAT, B.Com., F.C.A.,
Chartered Accountant

VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, PUTTUR D.K. 574 203

(A UNIT of VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR ®)

Income & Expenditure Account for the year ending 31-03-2020

Expenditure		Rs. Ps.	Income		Rs. Ps.
To Staff Salary:			By Tution and Other Fees		
Salary of Teaching Staff	6,10,00,917.00		Tution Fees	7,16,49,454.00	
Non-Teaching Staff	1,15,95,317.00		Specific Fees/Subscriptions:	3,73,19,137.00	
Menial Staff	7,89,649.00		Miscellaneous Fees:	5,23,515.00	
Gratuity	4,23,104.00	**7,38,08,987.00**	University Fees	1,00,70,609.00	11,95,62,715.00
To Specific Expenses:		38,53,749.00	By Miscellaneous Receipts		18,15,327.00
To Other Miscellaneous Payments: University Fees		96,88,918.00			
To Other Miscellaneous Payments		4,07,815.00	By Grants		10,93,235.00
To Contingencies		57,14,882.74	By NAIN INT. ON BANK A/C		10,428.00
To Consumables:		2,37,501.00	By ID Card		4,700.00
To Repairs and Maintance		20,22,085.00	By NCASEM 2019		2,57,800.00
To Alumni		72,974.00	By R&D MECHANICAL (PRIZE)		10,000.00
To CII MEMBERSHIP FEE		5,605.00			
To DEPT INFRASTRUCTURE		4,33,156.00	By Excess of Expenditure over income		51,51,033.44
To Unnath Bharath Abhiyan		48,223.00			
To ADMINISTATIVE OVERHEAD		67,300.00			
To ISTE Membership Fee (Remittance)		27,405.00			
To VTU E-shikshana		3,600.00			
To Meeting & Function Exps		40,245.00			
To ID Card		38,761.00			
KEA FEES		3,500.00			
KSCST STUDENT PROJECT		8,000.00			
RED CROSS EXP'S		8,220.00			
R&D MECHANICAL		39,684.00			
R&D E & C		35,933.00			
TECH SAMVRT 2019		56,510.00			
VIJNANA VIBHA		4,78,806.00			
VIVEKA SANKALPA		3,990.00			
E-TENDERING EXPENSES		21,000.00			
NAIN OPEX FUND		4,26,497.00			
Expenses on Grants received		21,57,307.60			
To Transferred to:					
Vivekananda Vidyavardhaka Sangha Puttur ®		2,30,49,638.10			
To Deperciation on:					
Furniture & Fittings	12,83,671.00				
Office Equipments	1,33,367.00				
Computers	19,23,159.00				
Lab Equipments	18,04,749.00	51,44,946.00			
		12,79,05,238.44			**12,79,05,238.44**

The following Expenditure related to Vivekananda College of Engineering & Technology are reflected in the Management Account i.e., Vivekananda Vidyavardhaka Sang

Particulars	Amount (Rs.)
1. Electricity Charges	45,65,085.00
2. Employees' Provident Fund - Employers' Share	33,02,543.00
3. Interest on Bank Loan	34,95,462.00
5. Deperciation on Buildings	1,61,28,795.00
Total Expenditure	2,74,91,885.00

Date: 16-10-2020
Place:Puttur

S. RAMA BHAT, B.Com. F.C.A.,
CHARTERED ACCOUNTANT

S. RAMA BHAT, B.Com., F.C.A.
A.P.M.C. Road
PUTTUR - 574 201
Mem. No. 012673
Chartered Accountant

VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, PUTTUR, D.K.

(A UNIT of VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR ®)

Balance Sheet As on 31-03-2020

Liabilities		Rs. Ps.	Assets		Rs. Ps.
Capital Fund:			Cash & Bank Balances:		
Opening Balance	3,88,90,857.65		Cash in Hand		13,757.60
Less: Excess of Expenditure over Income	51,51,033.44	3,37,39,824.21	Cash At Bank		
			State Bank of India:	85,933.00	
Advances and Refund			**Canara Bank (Nehru Nagar Branch)**		
As per Schedule		24,41,241.00	S.B.A/c No.64	34,953.16	
			S.B.A/c No.66	3,21,184.58	
Caution deposit			S.B.A/c No.742	51,473.00	
(ALB)	12,86,525.00		S.B.A/c No.784	12,10,028.00	
Add: Additions during the year	87,250.00		S.B.A/c No.1088	2,69,091.25	
	13,73,775.00		S.B.A/c No.6355	1,049.00	
Less: Paid during the year	.00	13,73,775.00	S.B.A/c No.6357	44,607.00	
			S.B.A/c No.6401	32,998.40	20,51,317.39
			Fixed Assets:		
Scholarships:			**Furniture & Fixtures**		
As per Last B/S	40,69,060.00		As per last B/s	1,17,72,144.23	
Received during the year	1,82,46,161.00		Add: During the year	10,64,570.00	
	2,23,15,221.00			1,28,36,714.23	
Less: Disbursed	1,74,50,096.00	48,65,125.00	Less: Depreciation 10%	12,83,671.00	1,15,53,043.23
Life Insurance Premium Payable		1,20,428.00	**Office Equipments**		
			As per last B/s	12,63,721.89	
			Add: During the year	69,950.00	
				13,33,671.89	
			Less: Depreciation 10%	1,33,367.00	12,00,304.89
	C/F	**4,25,40,393.21**		C/F	**1,48,18,423.11**

Contd....2

Liabilities		Rs. Ps.	Assets		Rs. Ps.
	B/F	**4,25,40,393.21**		B/F	**1,48,18,423.11**
TDS to be Remitted			**Library Books**		
As per last Balance Sheet	48,452.00		As per last B/s	1,24,30,327.40	
Add: Additions during the yea	1,24,083.00		Add: During the year	2,70,016.00	1,27,00,343.40
	1,72,535.00				
Less: Paid during the year	1,01,320.00	71,215.00	**Laboratory Equipments:**		
			As per last B/s	97,80,712.10	
			Add: During the year	22,50,948.00	
				1,20,31,660.10	
			Less: Depreciation @ 15%	18,04,749.00	1,02,26,911.10
			Computers		
			As per last B/s	35,03,873.00	
			Add: During the year	13,04,025.00	
				48,07,898.00	
			Less: Depreciation @ 60%	19,23,159.00	28,84,739.00
			TDS to be recoved		16,046.00
			TDS on Reciepts		
			As per last Balance Sheet	3,23,550.00	
			Less: Received during the year		
				3,23,550.00	
			Add: Additions during the year	1,12,549.60	4,36,099.60
			Advance and Refund (As per Schedule)		15,29,046.00
		4,26,11,608.21			**4,26,11,608.21**

Some of the Assets are reflected in the Parent Association i.e. VVS Puttur ®

Date: 16-10-2020
Place:Puttur

S. RAMA BHAT, B.Com., A.P.M.C. Road PUTTUR - 574 201 Mem. No. 012573 Chartered Accountant

S. Rama Bhat

S. RAMA BHAT, B.Com. F.C.A.,
CHARTERED ACCOUNTANT

Vivekananda College of Engineering & Technology, Puttur, D.K 574 203

(A UNIT of VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR ®)

RECEIPTS AND PAYMENTS ACCOUNTS FOR THE YEAR ENDING 31st MARCH 2021

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
To **Tuition and Other Fees**			**By Staff Salary and Allowances**		
a) **Tuition fee**		5,41,02,137.00	Salary of Teaching Staff	3,49,78,924.00	
b) **Specific fees:**			Non-Teaching Staff	86,08,825.00	
Annual College Fees	2,53,97,268.00		Menial Staff	7,62,105.00	4,43,49,854.00
Book Bank	15,75,167.00		**By** Gratuity Disbursed		49,07,506.00
Dept. Asso. Fee	4,94,200.00				
Graduation Day	2,09,250.00		**By Specific Expenses:**		
IOT Lab Fee	10,32,300.00		Co-curricular activities/Association	43,350.00	
Jnana Sangama	1,04,500.00		College Internal Examinations	3,22,059.00	
Lesson Plan	5,39,220.00		Graduation Day Exps	1,92,008.00	
Record Book	1,43,200.00		IOT Lab Exp's	19,820.00	
ID Card	4,400.00		Reading Room	99,083.00	
Training Fee	26,50,172.00	3,21,49,677.00	Sports Equipments/expenses	1,41,559.00	
c) **Miscellaneous Fees:**			Student Welfare	18,361.00	
Karnataka State Student Welfare Fund	30,750.00		ID Card	18,160.00	8,54,400.00
Karnataka State Teachers Benefit Fund	30,750.00				
National Foundation For Teachers Welfare	30,750.00		By **Other Miscellaneous Payments - University Fees**		
NSS Fee	48,800.00		Convocation Fees	3,68,000.00	
Red Cross	61,445.00		E-Learning fees	5,57,000.00	
Vidya Bharathi	20,050.00		Eligibility certificate fee	2,95,500.00	
Vidya Nidhi	2,42,400.00	4,64,945.00	Revaluation fees	2,35,940.00	
d) **Universtiy Fees**			Univ.Exam. Remuneration A/c	4,81,658.00	
E-Learning fees	5,44,500.00		University Examination fee	24,19,620.00	
Eligibility certificate fee	2,62,000.00		University Fees	10,72,350.00	
Revaluation fees	65,684.00		VTU Consortium Fee	9,98,000.00	
Univ.Exam. Remuneration A/c	3,13,898.19		VTU Registration Fee	7,09,000.00	
University Examination fee	28,91,162.00		VTU Exam Application	14,550.00	71,51,618.00
University Fees	10,46,297.00				
VTU Consortium Fee	10,30,250.00		**By Contingencies:**		
VTU Registration Fee	5,10,400.00	66,64,191.19	Advertisment / Publicity	70,563.00	
			Affiliation/Inspection fees	6,26,123.90	
To Interest on Bank Accounts	2,86,938.00		Bank Commission	10,033.39	
NAIN - Interest on SB A/C	834.00	2,87,772.00	Building Maintenance	46,421.00	
C/F		**9,36,68,722.19**	**C/F**	**7,53,141.29**	**5,72,63,378.00**

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
B/F		9,36,68,722.19	B/F	7,53,141.29	5,72,63,378.00
To Miscellaneous Receipts			Electrical Fittings and Wiring	1,07,419.00	
Admission Process Fee	1,28,220.00		Freight & Carriage	3,250.00	
Consultancy Civil	12,80,073.00		Institute Image Building (IIBC)	16,46,577.00	
Consultancy Mech	45,900.00		Internet Leased Line	3,21,550.00	
Fine & Miscellaneous Receipts	4,08,752.00		Miscellaneous Expenses	136.00	
Online Test Lab Charges	23,230.00		Office Automation Software	29,205.00	
Processing Charges	47,001.18		Photo Copier Expenses	32,805.00	
RV / Photo Copy Appl. Fee	260.00	19,33,436.18	Placement/Training	5,17,856.00	
			Postage, Telegram & Telephone	81,399.00	
To Scholarships			Printing & Stationery	8,05,623.00	
Fee Concession OBC Students	23,07,670.00		Professional charges	6,000.00	
Fee Concession SC/ST Students	11,92,050.00		RV / Photo Copy Appl. Fee	2,680.00	
Arivu Loan (Minority Dept.)	1,40,000.00	36,39,720.00	Staff Welfare	53,239.00	
			Travelling expenses	75,798.00	
To Grants			Online Class Software Expenses	2,12,400.00	
Grant KSCST	28,500.00		Meeting & Function Exps	18,370.00	
Grant - VTU	79,400.00		Software	17,000.00	46,84,448.29
Grant - NAIN	5,00,000.00				
NAIN Student Project Fund	10,00,000.00		By Consumables:		
NSS Grant	22,500.00		Chemistry	2,306.00	
Grant - AICTE	4,05,000.00	20,35,400.00	Civil	2,980.00	
To Advance and Refund (As per schedule)		12,64,168.60	Computer Science	7,340.00	
			Electronics	4,200.00	
To TDS - Others		92,817.00	IT Cell	2,88,740.00	
			Mechanical	17,096.00	3,22,662.00
To Caution Deposit		69,000.00	By Repairs and Maintance		
			General Repairs and Maintenance	64,920.00	
TO GST			Generator Maintenance	4,31,765.00	
CGST 9%	88,583.50		Maintenance of Premises	2,00,066.00	
SGST 9%	88,583.50	1,77,167.00	Maintenance of Vehicle	1,04,052.00	
			Repairs to Chem Lab equipmt.	5,487.00	
			Repairs to CS Lab equipmt.	12,150.00	
			Repairs to CV Lab equipmt.	1,835.00	
			Repairs to E & C Lab equipmt.	472.00	
			Repairs to IT Cell	43,979.00	
			Repairs to mba Lab equipmt.	200.00	
			Repairs to Mech. Lab equipmt.	46,544.00	9,11,470.00
C/F		10,28,80,430.97	C/F		6,31,81,958.29

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
B/F		10,28,80,430.97	B/F		6,31,81,958.29
To Salary Deductions			By **Scholarships**		
Employees Provident Fund	26,72,912.00		Fee Concession OBC Students	34,41,504.00	
ESI	57,918.00		Arivu Loan (Minority Dept.)	3,41,541.00	37,83,045.00
Labour Welfare Fund	2,980.00		By Consultancy Civil	7,14,513.00	
Life Insurance Premium	15,89,651.00		By CII MEMBERSHIP FEE	17,700.00	
Profession Tax	1,90,800.00		By DEPT INFRASTRUCTURE	11,000.00	
TDS	4,00,534.00		By KEA FEES	9,059.00	
STAFF LOAN - SCDC BANK (SHIVANANDA)	30,000.00	49,44,795.00	By KSCST STUDENT PROJECT	29,500.00	
			By R&D MECHANICAL	7,371.00	
			By R&D E & C	14,568.00	
			By KUPECA	85,000.00	8,88,711.00
			By **NAIN OPEX FUND**		
			Administrative Overhead	13,526.00	
			Bank Commission	590.00	
			NAIN - SALARY	3,54,000.00	
			NAIN Meeting Exp's	4,221.00	
			NAIN Mentors Expenditure	25,000.00	
			NAIN AUDIT FEES	2,000.00	3,99,337.00
			By **Grants**		
			Grant- VGST	2,39,372.00	
			Grant- VTU	42,690.00	
			Grant - EDII (GOVT.)	5,666.00	
			NSS Activity	1,360.00	2,89,088.00
			By **Laboratory Equipments:**		
			Civil	1,660.00	
			CS	1,06,130.00	
			IT Infrastructure	1,90,730.00	
			Office Equipment	20,299.00	3,18,819.00
			By Air Condition		2,80,000.00
			By Library Books		37,402.00
			By **Transferred to:**		
			Vivekananada Vidyavardhaka Sangha Puttur ®		2,71,93,418.10
			By GST		
			CGST 9%	31,035.00	
			SGST 9%	31,035.00	62,070.00
C/F		10,78,25,225.97	C/F		9,64,33,848.39

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
B/F	.00	10,78,25,225.97	B/F		9,64,33,848.39
			By Advance and Refund (As per schedule)		21,21,857.00
			By TDS - Other		67,347.00
			By TDS on Bills Receivable		33,655.45
			By **Salary Deductions**		
			Employees Provident Fund	26,72,912.00	
			ESI	57,918.00	
			Labour Welfare Fund	2,980.00	
			Life Insurance Premium	17,10,079.00	
			Profession Tax	1,90,800.00	
			TDS	4,00,534.00	
			STAFF LOAN - SCDC BANK (SHIVANANDA)	24,000.00	50,59,223.00
			By **Closing Balance**		
To Opening Balance			Cash in Hand	24,494.60	
Cash in Hand	13,757.60		**Cash at Bank**		
Cash at Bank			State Bank of India	88,294.00	
State Bank of India	85,933.00		Canara Bank S.B.A/c No.64	13,70,050.29	
Canara Bank S.B.A/c No.64	34,953.16		Canara Bank S.B.A/c No.66	5,20,917.58	
Canara Bank S.B.A/c No.66	3,21,184.58		Canara Bank S.B.A/c No.742	52,919.00	
Canara Bank S.B.A/c No.742	51,473.00		Canara Bank S.B.A/c No.784	12,88,320.00	
Canara Bank S.B.A/c No.784	12,10,028.00		Canara Bank S.B.A/c No.1088	7,51,269.25	
Canara Bank S.B.A/c No.1088	2,69,091.25		Canara Bank S.B.A/c No.6317	24,393.00	
Canara Bank S.B.A/c No.6355	1,049.00		Canara Bank S.B.A/c No.6355	9,90,648.00	
Canara Bank S.B.A/c No.6357	44,607.00		Canara Bank S.B.A/c No.6357	5,07,441.00	
Canara Bank S.B.A/c No.6401	32,998.40	20,65,074.99	Canara Bank S.B.A/c No.6401	5,55,623.40	61,74,370.12
		10,98,90,300.96			10,98,90,300.96

CORRESPONDENT

TREASURER

PRINCIPAL

AUDITOR'S CERTIFICATE

I certify that I have audited the Accounts of Vivekananda College of Engineering & Technology for the year ending on 31-03-2021 and that the Receipts and Payments shown in the above statement are correctly stated and supported by proper vouchers.

Place:Puttur
Date:

S. RAMA BHAT, B.Com., F.C.A.
A.P.M.C. Road
PUTTUR - 574 201
Mem. No. 012673
Chartered Accountant

S. Rama Bhat

S. RAMA BHAT, B.Com., F.C.A.,
Chartered Accountant

VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, PUTTUR D.K. 574 203

(A UNIT of VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR ®)

Income & Expenditure Account for the year ending 31-03-2021

Expenditure		Rs. Ps.	Income		Rs. Ps.
To Staff Salary:			**By Tution and Other Fees**		
Salary of Teaching Staff	3,49,78,924.00		Tution Fees	5,41,02,137.00	
Non-Teaching Staff	86,08,825.00		Specific Fees/Subscriptions:	3,21,49,677.00	
Menial Staff	7,62,105.00		Miscellaneous Fees:	4,64,945.00	
Gratuity	49,07,506.00	4,92,57,360.00	University Fees	66,64,191.19	9,33,80,950.19
To Specific Expenses:		8,54,400.00			
To Other Miscellaneous Payments: University Fees		71,51,618.00	By Miscellaneous Receipts		19,33,436.18
To Other Miscellaneous Payments					
To Contingencies		46,84,448.29	By Grants		20,35,400.00
To Consumables:		3,22,662.00			
To Repairs and Maintance		9,11,470.00	By Interest on Bank Accounts	2,86,938.00	
To Consultancy Civil		7,14,513.00	NAIN - Interest on SB A/C	834.00	2,87,772.00
CII MEMBERSHIP FEE		17,700.00			
DEPT INFRASTRUCTURE		11,000.00			
KEA FEES		9,059.00			
KSCST STUDENT PROJECT		29,500.00			
R&D MECHANICAL		7,371.00			
R&D E & C		14,568.00			
KUPECA		85,000.00			
NAIN OPEX FUND		3,99,337.00			
Expenses on Grant Received		2,89,088.00			
To Transferred to:					
Vivekananda Vidyavardhaka Sangha Puttur ®		2,71,93,418.10			
To Deperciation on:					
Furniture & Fittings	11,55,304.00				
Office Equipments	1,50,060.00				
Computers	12,72,640.00				
Lab Equipments	15,34,286.00	41,12,290.00			
To Excess of income over Expenditure		15,72,755.98			
		9,76,37,558.37			**9,76,37,558.37**

The following Expenditure related to Vivekananda College of Engineering & Technology are reflected in the Management Account i.e., Vivekananda Vidyavardhaka Sangl

Particulars	Amount (Rs.)
1. Electricity Charges	38,87,504.00
2. Employees' Provident Fund - Employers' Share	26,72,912.00
3. Interest on Bank Loan	23,13,196.00
5. Deperciation on Buildings	1,43,35,437.00
Total Expenditure	2,32,09,049.00

Date:
Place:Puttur

S. RAMA BHAT, B.Com. F.C.A.,
CHARTERED ACCOUNTANT

VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, PUTTUR, D.K.

(A UNIT of VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR ®)

Balance Sheet As on 31-03-2021

Liabilities		Rs. Ps.	Assets		Rs. Ps.
Capital Fund:			Cash & Bank Balances:		
Opening Balance	3,37,39,824.21		Cash in Hand		24,494.60
Add: Excess of Income			Cash At Bank		
over Expenditure	15,72,755.98	3,53,12,580.19	State Bank of India:	88,294.00	
			Canara Bank (Nehru Nagar Branch)		
Advances and Refund			S.B.A/c No.64	13,70,050.29	
As per Schedule		13,24,393.00	S.B.A/c No.66	5,20,917.58	
			S.B.A/c No.742	52,919.00	
Caution deposit			S.B.A/c No.784	12,88,320.00	
(ALB)	13,73,775.00		S.B.A/c No.1088	7,51,269.25	
Add: Additions during the year	69,000.00		S.B.A/c No.6317	24,393.00	
	14,42,775.00		S.B.A/c No.6355	9,90,648.00	
Less: Paid during the year	.00	14,42,775.00	S.B.A/c No.6357	5,07,441.00	
			S.B.A/c No.6401	5,55,623.40	61,49,875.52
Scholarships:			**Fixed Assets:**		
As per Last B/S	48,65,125.00		**Furniture & Fixtures**		
Received during the year	36,39,720.00		As per last B/s	1,15,53,043.23	
	85,04,845.00		Add: During the year		
Less: Disbursed	37,83,045.00	47,21,800.00		1,15,53,043.23	
			Less: Depreciation 10%	11,55,304.00	1,03,97,739.23
Life Insurance Premium Payable	1,20,428.00				
Less: Paid during the year	1,20,428.00	Nil	**Office Equipments**		
			As per last B/s	12,00,304.89	
GST Payable (to be transferred to VVS A/c)		1,15,097.00	Add: During the year	3,00,299.00	
				15,00,603.89	
			Less: Depreciation 10%	1,50,060.00	13,50,543.89
	C/F	**4,29,16,645.19**		C/F	**1,79,22,653.24**

Contd....2

Liabilities		Rs. Ps.	Assets		Rs. Ps.
	B/F	**4,29,16,645.19**		B/F	**1,79,22,653.24**
TDS to be Remitted			**Library Books**		
As per last Balance Sheet	71,215.00		As per last B/s	1,27,00,343.40	
Add: Additions during the yea	92,817.00		Add: During the year	37,402.00	1,27,37,745.40
	1,64,032.00				
Less: Paid during the year	67,347.00	96,685.00	**Laboratory Equipments:**		
			As per last B/s	1,02,26,911.10	
			Add: During the year	1,660.00	
				1,02,28,571.10	
			Less: Depreciation @ 15%	15,34,286.00	86,94,285.10
			Computers		
			As per last B/s	28,84,739.00	
			Add: During the year	2,96,860.00	
				31,81,599.00	
			Less: Depreciation @ 40%	12,72,640.00	19,08,959.00
			TDS to be recoved		16,046.00
			TDS on Reciepts		
			As per last Balance Sheet	4,24,870.00	
			Less: Received during the year		
				4,24,870.00	
			Add: Additions during the year	33,655.45	4,58,525.45
			Advance and Refund (As per Schedule)		12,75,116.00
		4,30,13,330.19			**4,30,13,330.19**

Some of the Assets are reflected in the Parent Association i.e. VVS Puttur ®

Date: 08-07-2015
Place:Puttur

S. Rama Bhat

S. RAMA BHAT, B.Com. F.C.A.,
CHARTERED ACCOUNTANT

S. RAMA BHAT, B.Com. F.C.A.
A.P.M.C. Road
PUTTUR - 574 201
Mem. No. 012673
Chartered Accountant

SCHEDULE NO. - 'A1'

VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R), PUTTUR, D.K. 574 203

SCHEDULE OF FIXED ASSETS AS ON 31-03-2021 - VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY

Sl. No.	Particulars	Balance as on 01-04-2020	Addiations during the year			Deletions during the year	Depreci-ation Rate	Depreciation	Balance as on 31-03-2021
			01-04-20 to 30-09-20	01-10-20 to 31-03-21	Total				
1	Vivekananda College of Engineering & Technology Main Building	25088496.05		2190000.00	2190000.00		10%	2618350.00	24660146.05
2	Vivekananda Ladies Hostel Building (New Block)	8388042.82					10%	838804.00	7549238.82
3	Vivekananda Boys Hostel Building (New Block-Nalanda)	21570807.87					10%	2157081.00	19413726.87
4	VCET Multi Purpose Technical Block Building	13159451.83					10%	1315945.00	11843506.83
5	V.V.S. Administrative Block Building	6582344.45					10%	658234.00	5924110.45
6	Gardening at VCET Campus	2360112.00							2360112.00
7	Street Lighting at College Campus	211273.00					15%	31691.00	179582.00
8	Compound Wall at College Campus	3661420.45					10%	366142.00	3295278.45
9	VCET Ring Road (Interlock road)	927612.00					10%	92761.00	834851.00
10	Land Development at College Campus	2649352.00							2649352.00
11	Road at College Campus	3104727.00					10%	310473.00	2794254.00
12	Furniture - Guest House & Administrative Block	762631.00					10%	76263.00	686368.00
13	Sewage Treatment Plant (STP) - Civil Works	2982469.00					10%	298247.00	2684222.00
14	Sewage Treatment Plant (STP) - Plant & Machinery	718136.00					15%	107720.00	610416.00
15	CC Camera at College Campus	81598.00					15%	12240.00	69358.00
16	Generator at VCET - 250 KVA	394150.00					15%	59123.00	335027.00
17	Generator Shed at VCET	70700.00					10%	7070.00	63630.00
18	Vehicle Shed at VCET	1010419.00					10%	101042.00	909377.00
19	Seminar Hall & Auditorium at VCET	50362384.00					10%	5036238.00	45326146.00
20	VCET Canteen Building (W.I.P)	5255908.00					10%	525591.00	4730317.00
		149342034.47	0.00	2190000.00	2190000.00			14613015.00	136919019.47

Puttur, D.K.
Date: 22-07-2019

S. Rama Bhat

S.RAMA BHAT, B.COM., F.C.A.,
CHARTERED ACCOUNTANT
AUDITOR

S. RAMA BHAT, B.Com., F.C.A.
A.P.M.C. Road
PUTTUR - 574 201
Mem. No. 012673
Chartered Accountant

Vivekananda College of Engineering & Technology, Puttur, D.K 574 203

(A UNIT of VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR ®)

RECEIPTS AND PAYMENTS ACCOUNTS YEAR ENDING 31ST MARCH 2022 ((Provisional)

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
To **Tuition and Other Fees**			**By Staff Salary and Allowances**		
a) **Tuition fee**		6,17,53,349.00	Salary of Teaching Staff	4,58,94,881.00	
b) **Specific fees:**			Non-Teaching Staff	1,02,63,035.00	
Annual College Fees	2,58,82,691.72		Menial Staff	7,69,673.00	
Book Bank	14,46,000.00		Gratuity	23,33,133.00	5,92,60,722.00
Dept. Asso. Fee	4,64,705.00				
Graduation Day	2,46,750.00		**By Specific Expenses:**		
IOT Lab Fee	10,30,800.00		Book Bank	2,24,188.00	
Jnana Sangama	93,250.00		Co-curricular activities/Association	1,86,461.59	
Lesson Plan	5,18,200.00		Graduation Day Exps	2,85,945.00	
Record Book	1,42,300.00		IOT Lab Exp's	3,800.00	
Training Fee	24,33,533.00		Red Cross Exp's	750.00	
Skill lab fee	19,10,574.00	3,41,68,803.72	Library Books	1,68,070.00	
c) **Miscellaneous Fees:**			Reading Room	94,715.00	
Karnataka State Student Welfare Fund	28,950.00		Sports Equipments/expenses	94,312.00	
Karnataka State Teachers Benefit Fund	28,940.00		Student Welfare	1,37,337.00	11,95,578.59
National Foundation For Teachers Welfare	28,930.00				
NSS Fee	44,486.00				
Red Cross	56,590.00		By **Other Miscellaneous Payments - University Fees**		
Vidya Bharathi	25,675.00		Change of Branch	11,000.00	
Vidya Nidhi	2,22,800.00	4,36,371.00	Convocation Fees	3,00,000.00	
d) **Universtiy Fees**			E-Learning fees	88,000.00	
Change of Branch	10,020.00		Eligibility certificate fee	58,000.00	
E-Learning fees	5,37,500.00		Univ.Exam. Remuneration A/c	3,60,805.00	
Eligibility certificate fee	2,82,500.00		University Examination fee	17,39,457.70	
Revaluation fees	6,81,908.00		University Fees	7,72,950.00	
Univ.Exam. Remuneration A/c	3,58,251.00		VTU Consortium Fee	7,20,750.00	
University Examination fee	25,71,143.00		VTU Registration Fee	1,80,500.00	
University Fees	10,26,750.00		VTU Exam Application	8,530.00	
VTU Consortium Fee	9,81,750.00		KEA Fees	22,500.00	42,62,492.70
VTU Registration Fee	9,88,060.00	74,37,882.00			
C/F		**10,37,96,405.72**	**C/F**		**6,47,18,793.29**

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
B/F		10,37,96,405.72	B/F	.00	6,47,18,793.29
To **Miscellaneous Receipts**			**By Contingencies:**		
Admission Process Fee	1,09,210.00		Advertisment / Publicity	2,10,767.00	
Consultancy Civil	9,67,749.00		Affiliation/Inspection fees	8,50,000.00	
Consultancy Mech	25,530.00		Bank Commission	19,722.05	
Fine & Miscellaneous Receipts	4,76,319.00		Building Maintenance	2,04,020.00	
Intrest on Bank Accounts	1,52,228.00		Electrical Fittings and Wiring	3,12,803.00	
Online Test Lab Charges	1,02,828.20		Freight & Carriage	5,070.00	
Processing Charges	25,000.00	18,58,864.20	Institute Image Building (IIBC)	3,94,854.00	
			Internet Leased Line	11,63,883.00	
To Scholarships			Miscellaneous Expenses	2,430.00	
Fee Concession SC/ST Students	47,05,090.00		Office Automation Software	29,205.00	
Arivu Loan (Minority Dept.)	3,60,000.00	50,65,090.00	Photo Copier Expenses	71,365.00	
			Placement/Training	7,90,424.00	
To Salary Deductions			Postage, Telegram & Telephone	83,840.00	
Employees Provident Fund	29,11,021.00		Printing & Stationery	80,334.00	
ESI	80,880.00		Professional charges	6,150.00	
Labour Welfare Fund	3,100.00		Staff Welfare	14,395.00	
Life Insurance Premium	14,81,608.00		Travelling expenses	93,415.00	
Profession Tax	2,72,200.00		Fire & Safty	18,372.00	43,51,049.05
TDS	10,05,890.00	57,54,699.00			
			By Consumables:		
To Grants			Chemistry	38,045.00	
Grant KSCST	34,500.00		Civil	81,067.00	
Grant - VTU	40,000.00		Computer Science	1,59,000.00	
Grant - NAIN	3,20,000.00		Electronics	44,973.00	
Grant Other	2,00,000.00		IT Cell	1,95,690.00	
Grant - VGST	93,000.00	6,87,500.00	Mechanical	6,931.00	
			Physics	1,900.00	
To Advance and Refund (as per schdule)		12,15,856.00	AI	27,612.00	5,55,218.00
To TDS - Others		24,388.00			
To ID Card		16,494.72	By **Repairs and Maintenance**		
To Caution Deposit		1,29,850.00	General Repairs and Maintenance	44,531.00	
TO GST			Generator Maintenance	6,09,273.00	
CGST 9%	88,435.00		Maintenance of Premises	3,97,365.00	
SGST 9%	88,579.00	1,77,014.00	Maintenance of Vehicle	92,723.00	
C/F		11,87,26,161.64	C/F	11,43,892.00	6,96,25,060.34

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
B/F		11,87,26,161.64	B/F	11,43,892.00	6,96,25,060.34
To NAIN INT. ON BANK A/C		5,765.00	Repairs to Chem Lab equipmt.	610.00	
			Repairs to CV Lab equipmt.	40,478.00	
To Alumni Fees		1,65,001.00	Repairs to IT Cell	85,621.00	
To NSS Activity		1,874.00	Repairs to mba Lab equipmt.	5,860.00	
			Repairs to Mech. Lab equipmt.	15,326.00	12,91,787.00
To Department Association Account					
Association of Electronics & Communication	1,25,000.00		By Scholarships		
Association of Computer Science	75,000.00		Scholarships Other	2,09,350.00	
Association of Management Studies	75,000.00		Fee Concession SC/ST Students	44,03,917.00	
Civil Engg. Student Association	4,72,000.00		Arivu Loan (Minority Dept.)	3,60,000.00	49,73,267.00
Mechanical Engg. Student Association	4,00,000.00				
FY Student Association	1,25,000.00	12,72,000.00	By Laboratory Equipments:		
			AI	27,28,636.00	
			CV	15,111.00	
			EC	2,06,471.00	
			CS	59,08,000.00	
			IT Infrastructure	7,25,746.00	
			MCA	24,55,292.00	1,20,39,256.00
			By Adv. & Refund		6,66,814.00
			By Furniture/Fixture		12,90,357.00
			By Consultancy Civil		13,24,216.00
			By TDS - Other		1,03,288.00
			By CII MEMBERSHIP FEE		17,700.00
			By DEPT INFRASTRUCTURE		16,910.00
			By **Salary Deductions**		
			Employees Provident Fund	29,11,021.00	
			ESI	80,880.00	
			Labour Welfare Fund	3,100.00	
			Life Insurance Premium	14,82,301.00	
			Profession Tax	2,72,200.00	
			TDS	10,05,890.00	57,55,392.00
			By **Transferred to:**		
			Vivekananada Vidyavardhaka Sangha Puttur ®		2,06,41,911.00
			By **Grants**		
			Grant- KSCST	45,500.00	

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
C/F		12,01,70,801.64	C/F	45,500.00	11,77,45,958.34
B/F	.00	12,01,70,801.64	B/F	45,500.00	11,77,45,958.34
			Grant- VTU	40,000.00	
			Grant - EDII (GOVT.)	280.00	
			NSS Activity	660.00	
			AICTE	93,000.00	1,79,440.00
			By ADMINISTATIVE OVERHEAD		1,566.00
			By Software		2,15,340.00
			By Workshop/Seminar		5,791.00
			BY Website		1,16,125.00
			By KSCST STUDENT PROJECT		500.00
			By R&D MECHANICAL		20,000.00
			By R&D E & C		1,000.00
			By ISTE Membership Fee		42,480.00
			By GST		
			CGST 9%	1,41,710.00	
			SGST 9%	1,41,710.00	2,83,420.00
			By NAIN		
			NAIN - SALARY	3,54,000.00	
			NAIN Student Project Fund	9,16,561.00	
			NAIN INT. ON BANK A/C	19,756.00	12,90,317.00
			By Department Association Account		
			Association of Electronics & Communication	3,36,600.00	
			Association of Computer Science	8,39,100.00	
			Association of Management Studies	22,000.00	
			Civil Engg. Student Association	1,83,600.00	
			Mechanical Engg. Student Association	8,92,470.00	
			FY Student Association		22,73,770.00
C/F		12,01,70,801.64	C/F		12,21,75,707.34

RECEIPTS	Amount (Rs.)		PAYMENTS	Amount (Rs.)	
B/F	.00	12,01,70,801.64	B/F		12,21,75,707.34
To Opening Balance			By Closing Balance		
Cash in Hand	24,494.60		Cash in Hand	17,247.60	
Cash at Bank			**Cash at Bank**		
State Bank of India	88,294.00		State Bank of India	90,102.00	
Canara Bank S.B.A/c No.64	13,70,050.29		Canara Bank S.B.A/c No.64	3,49,208.95	
Canara Bank S.B.A/c No.66	5,20,917.58		Canara Bank S.B.A/c No.66	15,62,653.22	
Canara Bank S.B.A/c No.742	52,919.00		Canara Bank S.B.A/c No.742	54,352.00	
Canara Bank S.B.A/c No.784	12,88,320.00		Canara Bank S.B.A/c No.784	6,92,346.00	
Canara Bank S.B.A/c No.1088	7,51,269.25		Canara Bank S.B.A/c No.1088	6,31,089.25	
Canara Bank S.B.A/c No.6317	24,393.00		Canara Bank S.B.A/c No.6317	25,108.00	
Canara Bank S.B.A/c No.6355	9,90,648.00		Canara Bank S.B.A/c No.6355	79,202.00	
Canara Bank S.B.A/c No.6357	5,07,441.00		Canara Bank S.B.A/c No.6357	96,243.00	
Canara Bank S.B.A/c No.6401	5,55,623.40	61,74,370.12	Canara Bank S.B.A/c No.6401	5,71,912.40	41,69,464.42
		12,63,45,171.76			12,63,45,171.76

CORRESPONDENT

TREASURER

PRINCIPAL

Place:Puttur
Date: 01-06-2022

S. RAMA BHAT, B.Com., F.C.A.,
Chartered Accountant

S. RAMA BHAT, B.Com., F.C.A.
A.P.M.C. Road
PUTTUR - 574 201
Mem. No. 012573
Chartered

VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, PUTTUR D.K. 574 203

(A UNIT of VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR ®)

Income & Expenditure Account for the year ending 31-03-2022 (Provisional)

Expenditure		Rs. Ps.	Income		Rs. Ps.
To Staff Salary:			**By Tution and Other Fees**		
Salary of Teaching Staff	4,58,94,881.00		Tution Fees	6,17,53,349.00	
Non-Teaching Staff	1,02,63,035.00		Specific Fees/Subscriptions:	3,41,68,803.72	
Menial Staff	7,69,673.00		Miscellaneous Fees:	4,36,371.00	
Gratuity	23,33,133.00	5,92,60,722.00			
			University Fees	74,37,882.00	10,37,96,405.72
To Specific Expenses:		9,71,390.59			
To Other Miscellaneous Payments: University Fees		42,62,492.70	By Miscellaneous Receipts		18,58,864.20
To Other Miscellaneous Payments					
To Contingencies		43,51,049.05	By Grants		6,87,500.00
To Consumables:		5,55,218.00			
To Repairs and Maintance		12,91,787.00	By ID Card		16,494.72
To Consultancy Civil		13,24,216.00	By NAIN INT. ON BANK A/C		5,765.00
To CII MEMBERSHIP FEE		17,700.00	By Alumni Fees		1,65,001.00
To DEPT INFRASTRUCTURE		16,910.00	By NSS Activity		1,874.00
To ADMINISTATIVE OVERHEAD		1,566.00	By Department Association Account		12,72,000.00
To Software		2,15,340.00			
To Workshop/Seminar		5,791.00			
To Website		1,16,125.00			
To KSCST STUDENT PROJECT		500.00			
To R&D MECHANICAL		20,000.00			
To R&D E & C		1,000.00			
To ISTE Membership Fee		42,480.00			
Expenses on Grant Received		1,79,440.00			
NAIN Projects Expenses		12,90,317.00			
Department Association Account Expenses		22,73,770.00			
To Transferred to:					
Vivekananda Vidyavardhaka Sangha Puttur ®		2,06,41,911.00			
To Deperciation on:					
Furniture & Fittings	11,68,810.00				
Office Equipments	1,35,054.00				
Computers	82,35,980.00				
Lab Equipments	13,37,380.00	1,08,77,224.00			
To Excess of income over Expenditure		86,955.30			
		10,78,03,904.64			**10,78,03,904.64**

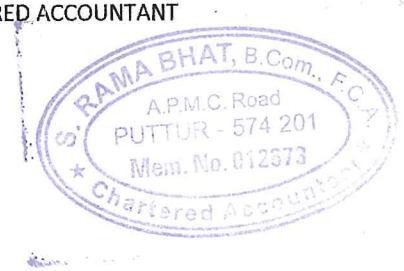
contd...2

The following Expenditure related to Vivekananda College of Engineering & Technology are reflected in the Management Account i.e., Vivekananda Vidyavardhaka Sangha Puttur (R)

Particulars	Amount (Rs.)
1. Electricity Charges	38,29,214.00
2. Employees' Provident Fund - Employers' Share	29,11,021.00
3. Interest on Bank Loan	44,21,596.00
5. Deperciation on Buildings	1,32,57,426.00
Total Expenditure	2,44,19,257.00

Date: 01-06-2022
Place:Puttur

S. RAMA BHAT, B.Com. F.C.A.,
CHARTERED ACCOUNTANT



VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, PUTTUR, D.K.

(A UNIT of VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR ®)

Balance Sheet As on 31-03-2022 (Provisional)

Liabilities		Rs. Ps.	Assets		Rs. Ps.
Capital Fund:			Cash & Bank Balances:		
Opening Balance	3,53,12,580.19		Cash in Hand		17,247.60
Less: Excess of Expenditure			Cash At Bank		
over Income	86,955.30	3,53,99,535.49	State Bank of India:	90,102.00	
			Canara Bank (Nehru Nagar Branch)		
Advances and Refund			S.B.A/c No.64	3,49,208.95	
As per Schedule		19,43,018.00	**S.B.A/c No.66**	15,62,653.22	
			S.B.A/c No.742	54,352.00	
Caution deposit			**S.B.A/c No.784**	6,92,346.00	
(ALB)	14,42,775.00		S.B.A/c No.1088	6,31,089.25	
Add: Additions during the year	1,29,850.00		S.B.A/c No.6317	25,108.00	
	15,72,625.00		S.B.A/c No.6355	79,202.00	
Less: Paid during the year	.00	15,72,625.00	S.B.A/c No.6357	96,243.00	
			S.B.A/c No.6401	5,71,912.40	41,52,216.82
Scholarships:			**Fixed Assets:**		
As per Last B/S	47,21,800.00		**Furniture & Fixtures**		
Received during the year	50,65,090.00		As per last B/s	1,03,97,739.23	
	97,86,890.00		Add: During the year	12,90,357.00	
Less: Disbursed	49,73,267.00	48,13,623.00		1,16,88,096.23	
			Less: Depreciation 10%	11,68,810.00	1,05,19,286.23
GST Payable (to be transferred to VVS A/c)			**Office Equipments**		
As per Last B/s	1,15,097.00		As per last B/s	13,50,543.89	
Add: Additions during the year	1,77,014.00		Add: During the year		
	2,92,111.00			13,50,543.89	
Less: Paid during the year	2,83,420.00	8,691.00	Less: Depreciation 10%	1,35,054.00	12,15,489.89
	C/F	**4,37,37,492.49**		C/F	**1,59,04,240.54**

Contd....2

Liabilities		Rs. Ps.	Assets		Rs. Ps.
	B/F	**4,37,37,492.49**		B/F	**1,59,04,240.54**
TDS to be Remitted			**Library Books**		
As per last Balance Sheet	96,685.00		As per last B/s	1,27,37,745.40	
Add: Additions during the yea	24,388.00		Add: During the year	2,24,188.00	1,29,61,933.40
	1,21,073.00				
Less: Paid during the year	1,03,288.00	17,785.00	**Laboratory Equipments:**		
			As per last B/s	86,94,285.10	
			Add: During the year	2,21,582.00	
				89,15,867.10	
			Less: Depreciation @ 15%	13,37,380.00	75,78,487.10
			Computers		
			As per last B/s	19,08,959.00	
			Add: During the year	1,18,17,674.00	
				1,37,26,633.00	
			Less: Depreciation @ 40%	82,35,980.00	54,90,653.00
			TDS to be recoved		16,046.00
			TDS on Reciepts		
			As per last Balance Sheet	4,58,525.45	
			Less: Received during the year		
				4,58,525.45	
			Add: Additions during the year		4,58,525.45
			Life Insurance Premium to be recovered		693.00
			Advance and Refund (As per Schedule)		13,44,699.00
		4,37,55,277.49			**4,37,55,277.49**

Some of the Assets are reflected in the Parent Association i.e. VVS Puttur ®

Date: 01-06-2022
Place:Puttur

S. RAMA BHAT, B.Com., A.C.
A.P.M.C. Road
PUTTUR - 574 201
Mem. No. 012673
Chartered Accountant

S. Rama Bhat

S. RAMA BHAT, B.Com. F.C.A.,
CHARTERED ACCOUNTANT

अखिल भारतीय तकनीकी शिक्षा परिषद्
ALL INDIA COUNCIL FOR TECHNICAL EDUCATION
(भारत सरकार का एक सांविधिक संस्थान) (A STATUTORY BODY OF THE GOVERNMENT OF INDIA)

F.No.: 770-53-055(NDEG)/ET/2001
Date : August 24, 2001

To
Secretary, Education Department
Govt. of Karnataka,
M.S. Building
Bangalore – 560 001.

Sub: AICTE approval to **PUTTUR EDUCATIONAL TRUST ® PUTTUR, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST. KARNATAKA** for establishment of New Degree Engg. College under the Name & Style of **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST. KARNATAKA.**

Sir,

I am directed to state that based on the consultations with the concerned State Govt., the concerned affiliating body and on recommendations of the Regional Committee, the Expert Committee constituted by the Council and as per the provisions of AICTE Act and Regulations, the All India Council for Technical Education (AICTE), is pleased to accord approval to PUTTUR EDUCATIONAL TRUST ® PUTTUR, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST. KARNATAKA for establishment of New Degree Engg. College under the Name & Style of VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST. KARNATAKA. for the academic year 2001-2002, for course(s) and intake as given below with specific condition that admission shall be made through the Central Counseling by the Government of Karnataka only. This approval is valid only for the academic years 2001-2002 and cannot be extended for the next year 2002-2003. In the event the establishment of the institutions having not been operationalised, this approval is not valid unless AICTE specifically revalidates.

COURSE(S)	INTAKE	LEVEL	DURATION (YEARS)	PERIOD OF APPROVAL
1. COMPUTER SCIENCE & ENGG.	50.	DEGREE	4	2001-2002
2. INFORMATION TECHNOLOGY	50.	DEGREE	4	2001-2002
3. ELECTRONICS & COMM. ENGG.	50.	DEGREE	4	2001-2002

This approval has been accorded subject to fulfillment of general conditions and as per the Norms and Standards of the AICTE, and also specific conditions(if any, given).

The attention of the management is drawn to the fact that the approval given now is only for one academic session before the end of which an expert committee shall visit to assess if the norms and standards as stipulated by AICTE are fulfilled, and only then will the continuation or otherwise shall be intimated.

The admission will be made in accordance with Regulations notified by the AICTE vide GSR 476(E) dated 20.05.1994 based on the Hon'ble Supreme Court Judgement dated 04.02.1993 with regard to WP(C) No. 607 of 1992 in the case of Unni Krishanan JP and other etc. V/s. State Government of Andhra Pradesh and others etc. and later judgements. No Management/Institute/Trust or Society shall announce admissions directly under any circumstances. Any action by the institute contrary to any provisions laid down by the Council and concerned State Government shall make it liable for actions.

Contd\2...

In the event of infringement/contravention or non-compliance of the provisions of AICTE Regulations, Guidelines or the norms and standards as prescribed by the AICTE, the Council shall take further action to withdraw approval, and the liability arising out of such withdrawal of approval will be solely that of Management/Trust/Society and/or Institution.

The Council may inspect/ visit the Institution any time it may deem fit to verify the progress/ compliance.

You are requested to kindly monitor the progress made by this institution towards fulfilling the norms and standards prescribed by the Council and keep the concerned Regional Office and AICTE, New Delhi informed.

Yours faithfully,

(Dr. P.N. Razdan)
Adviser (E&T)

Copy to :

1. The Regional Officer, AICTE, SWRO, Bangalore University Campus, Palace Road, Bangalore – 560 019.

He is requested to monitor compliance with the Norms and Standards and conditions stipulated by the Council and keep the concerned Regional Committee and the AICTE informed of the same.

He is also requested to ensure the receipt of notorised undertaking as specified by the Council from the institution/management concerned within the stipulate time frame.

2. The Director of Technical Education, Govt. Karnataka, Palace Road, Bangalore – 560 001.

3. The Registrar,

He is requested to complete the process of affiliation for facilitating admissions.

4. The Principal, **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST. KARNATAKA.**

(i)The institution should submit a notorised undertaking on non-judicial stamp paper as per format given in Annexure I to the concerned Regional Office, AICTE with a copy to the Headquarters, AICTE, New Delhi within one month from the date of receipt of this approval letter.

(ii)The institution/management should also submit a notorised undertaking from the Governing Body to the concerned Regional Office, AICTE with a copy to Headquarters, AICTE, New Delhi and to the concerned State Government, that all the infrastructural and instructional facilities shall be in place as per the norms of AICTE prior to the admissions of any student for the academic year 2001-2002.

5. Guard File

(Dr. P.N. Razdan)
Adviser (E&T)

अखिल भारतीय तकनीकी शिक्षा परिषद्
ALL INDIA COUNCIL FOR TECHNICAL EDUCATION
(भारत सरकार का एक सांविधिक संस्थान) (A STATUTORY BODY OF THE GOVERNMENT OF INDIA)

S.NO. 80.
F.No:770-53-296(E)/ET/2001
Date: 05-06-2002

To

The Secretary Education Dept.,
Govt. of Karnataka, M S Building,
Bangalore – 560 001.
Karnataka.

Subject: Increase in Intake/ Additional Course/ Extension of Approval, to **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY,, NEHRU NAGAR,, PUTTUR TALUK, DAKSHINA KANNADA DIST., KARNATAKA,** , for conduct of **DEGREE** programmes.

Sir,

I am directed to state that the All India Council for Technical Education (AICTE), is pleased to accord extension of approval to **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY,, NEHRU NAGAR,, PUTTUR TALUK, DAKSHINA KANNADA DIST., KARNATAKA,** , for the course(s) and intake capacity as given below with the specific conditions that admission shall be made through the Central Counseling by the Govt. of **KARNATAKA** only:

COURSE (S)	PREVIOUS APPROVED INTAKE	REVISED APPROVED INTAKE	PERIOD OF APPROVAL
COMPUTER SC. & ENGINEERING	50	60	2002-2003
ELECTRONICS & COMM ENGINEERING	50	60	2002-2003
INFORMATION TECHNOLOGY	50	60	2002-2003
TOTAL	150.	180.	

This approval has been accorded subject to fulfillment of specific conditions listed at Annexure- I (if any) and Norms and Standards & General Conditions as stipulated by Council in Annexure-II.

Further, in the event of infringement/contravention or non-compliance of the norms & standards prescribed by the AICTE during the last approved academic year, the Council shall take further action to withdraw approval to this case for admission during subsequent academic year and the liability arising out of such withdrawal of approval will be solely that of Management / Trust /Society and/or institutions.

Contd...2/-

इंदिरा गांधी खेल परिसर, इन्द्रप्रस्थ एस्टेट, नई दिल्ली – 110 002
Indira Gandhi Sports Complex, I.P. Estate, New Delhi-110 002
दूरभाष/Phone : 3399010/11/12/13/15/16/17/18, फैक्स/Fax : 011-3399002

S.NO. 80.
F.No:770-53-296(E)/ET/2001

The Council reserves the right to visit the Institution any time it may deem fit to verify the compliance of norms and standards of AICTE.

You are requested to kindly monitor the progress made by this institution for fulfillment of the norms & standards of the Council & keep the concerned Regional Committee and AICTE informed.

Yours faithfully,

(P.N.RAZDAN)
ADVISER (UG)

copy to:

1. The Regional Officer, AICTE South Western Regional Regional Officer, Health Centre Building, Bangalore University Campus, Bangalore - 560 009.

   He is requested to monitor compliance with the norms & standards and conditions stipulated by the Council and keep the concerned Regional Committee and the AICTE informed of the same.

   He is also requested to ensure the receipt of notorised undertaking as specified by the Council from the institution / management concerned within the stipulate time frame.

2. The Director of Technical Education,
   Govt. of Karnataka, Palace Road,
   Bangalore – 560 001.

3. The Registrar, VISVESHWARAIAH TECHNOLOGICAL UNIVERSITY.
   He is requested to complete the process of affiliation for facilitating admissions.

4. The Principal,
   VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY,,
   NEHRU NAGAR,, PUTTUR TALUK, DAKSHINA KANNADA DIST.,
   KARNATAKA,,

5. Guard File.

Razdan

(P.N.RAZDAN)
ADVISER (UG)

Annexure - I

F.No. 770-53-262(E)/ET/96

NAME OF THE INSTITUTION	COURSE / PROGRAMME
Vivekananda Institute of Technology Gudimavu Village, Kengeri Hobli, Near Kumbalgodu. Bangalore - 560 074	DEGREE IN ENGINEERING & TECHNOLOGY

SPECIFIC CONDITIONS (THE SPECIFIC CONDITIONS SHOULD BE FULFILLED BY 30TH SPET., AND A REPORT SHOULD BE SUBMITTED TO THE CONCERNED REGIONAL OFFICE WITH A COPY TO HEAD QUARTER) ::

1) The infrastructure facilities in terms of Library, Laboratory, Computer Center and Class Room should be augmented as per AICTE norms.

2) More senior faculty with appropriate experience and qualifications should be added to meet the Norms of AICTE. AICTE pay scales should be implemented at the earliest.

(A.K. Nassa)
Dy. Director (UG)

अखिल भारतीय तकनीकी शिक्षा परिषद्
ALL INDIA COUNCIL FOR TECHNICAL EDUCATION

(भारत सरकार का एक सांविधिक संस्थान) (A STATUTORY BODY OF THE GOVERNMENT OF INDIA)

S.No. 1

F.No.:

Date:12.06.2003

20/6/03

To

The Secretary
Education Department
Govt. of Karnataka
M.S. Building, Bangalore – 560 001
KARNATAKA.

Sub: Extension of approval of AICTE to VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR, D.K. - 574 203, KARNATAKA for the academic year 2003-04.

Sir/Madam,

The Application/ Proposal and/ or the Compliance Report received from **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR, D.K. - 574 203, KARNATAKA,** has been processed as per laid down procedure, guidelines, policy and/or norms & standards of AICTE, mentioned in **AICTE Regulations and/ or "AICTE Hand Book for Approval Process".**

I am directed to state that the All India council for Technical Education (AICTE) is pleased to accord approval to **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR, D.K. - 574 203, KARNATAKA,** for extension of AICTE Approval/ Introduction of new course(s)/ Variation in intake (Increase/ Decrease), as applicable for **under-graduate degree level course(s) in Engineering /Technology** with annual intake for each course as given below :

FULL TIME COURSE(S)	EXISTING ANNUAL INTAKE	REVISED APPROVED INTAKE	ENTRY LEVEL	DURATION (YEARS)	PERIOD OF APPROVAL
COMPUTER SC & ENGG.	60	45	10+2	4	2003-2004
ELECTRONICS & COMMUNICATION ENGG.	60	45	10+2	4	2003-2004
INSTRUMENTATION ENGG.	60	45	10+2	4	2003-2004
Total Annual Intake	**180**	**135**			

Received.

Mysore

इंदिरा गांधी खेल परिसर, इन्द्रप्रस्थ एस्टट, नई दिल्ली – 110002
Indira Gandhi Sports Complex, I.P. Estate, New Delhi-110002
दूरभाष / Phone : 23392506, 63-65,68,71,73-75 फैक्स / Fax : 011-23392554

The approval accorded above is subject to fulfillment of the following Conditions:

1. All full time faculty members as per AICTE Norms must be recruited before making admissions.

2. The Institution must have Affiliation to a University for the above courses before making admissions. In the absence of such Affiliation, this Letter of approval shall be treated as Withdrawn. **(Order of the High Court of Madras in W.P. No. 33256 of 2002 and other Batch of Petitions).**

3. All the required Laboratories/ Workshops/ Machineries/ Equipment, as per approved syllabi of the affiliating University, must be operational before making admissions.

4. The approved course(s) shall commence as per the academic calendar of the Affiliating University.

5. If this Letter of approval is received by you after the closing date of State / National Level Central Counseling for Admissions in the concerned State / Union Territory, this Letter of approval will not be valid for making any admission during the above specified academic year, and shall be treated as withdrawn.

6. No excess admission shall be made by the Institution during any academic year.

7. The approval is valid only for the academic year 2003-2004. If no further extension of AICTE approval is received beyond the academic year 2003-2004, this Approval Letter will not be valid for making any admission for the subsequent years.

8. Name of the Institution, Name of the Society/Trust, are not allowed to be changed without prior approval of AICTE. The name and title of the institution should be such that "**the Emblems and Names (Prevention of improper use) Act 12 (1950)**" of Government of India, is not violated in any manner.

   The use of word "Indian" and /or "National" and/or "All India" and/or "All India Council" and/or Commission" in any part of the name of a Technical Institution and/ or any name whose abbreviated form leads to "IIM"/ "IIT"/"IISC"/"IIIT"/ "AICTE"/ "UGC" shall not be permitted. These restrictions will not be applicable for those institutions which are established with the name approved by the Govt. of India.

9. In exercise of power conferred under 10(p) of the AICTE Act, AICTE, may inspect the Institution any time it may deem fit to verify the progress/ compliance or for any other purpose.

10. Any other condition(s) as may be specified by AICTE from time to time.

It may please be noted that consequent to judgement of Hon'ble Supreme Court delivered on 31/10/2002 in TMA Pai Case, the AICTE had issued interim policy regulations, which has been notified in the Gazette of India on 20/03/2003. All the provisions contained in the interim policy regulations shall be applicable for the academic year 2003-2004 in respect of all the AICTE approved institutions.

Contd 3

In the event of infringement/ contravention or non-compliance of the above Conditions and/or the provision of AICTE Act & Regulations/ Guidelines/ Norms & Standards as prescribed by AICTE, further actions leading to 'Reduced Intake' or "No Admission or Withdrawal of Approval, may be taken by AICTE and the liability arising out of such actions will be solely that of the Management of the Institution.

Your faithfully,

(Prof. R.S. Gaud)
Adviser (UG)

Copy to:

1. The Regional Officer,
   AICTE , South Western Regional Office
   Health Centre Building
   Bangalore University Campus
   Bangalore – 560 009.

2. The Registrar, **VISVESWARAIAH TECHNOLOGICAL UNIVERSITY.**

3. The Principal
   VIVEKANANDA COLLEGE OF ENGINEERING
   & TECHNOLOGY,
   NEHRU NAGAR,
   PUTTUR, D.K. - 574 203,
   KARNATAKA

4. The Director of Technical Education
   Govt. of Karnataka,
   Palace Road,
   Bangalore – 560 001.

5. Guard File, Bureau (UG).

अखिल भारतीय तकनीकी शिक्षा परिषद्
ALL INDIA COUNCIL FOR TECHNICAL EDUCATION

(भारत सरकार का एक सांविधिक निकाय) (A STATUTORY BODY OF THE GOVT. OF INDIA)

F.No. 770-53-262(E)/ET/96
September 28, 2004

To,
The Secretary Education Department
Govt. of Karnataka
M.S. Building, Bangalore - 560 001
KARNATAKA.

Subject: **Extension of approval of AICTE to Vivekananda College of Engineering & Technology, Nehru Nagar, Puttur, D.K. - 574 203 for the academic year 2004-2005.**

Sir / Madam,

This is in continuation of our letter cited on the same subject for the institution mentioned above. The Application / Proposal and / or the Compliance Report Received from **Vivekananda College of Engineering & Technology, Nehru Nagar, Puttur, D.K. - 574 203,** has been processed as per laid down procedure, guidelines, policy and / or norms and standards of AICTE, mentioned in AICTE Regulations and / or "AICTE Hand Book for Approval Process".

I am directed to state that the All India Council for Technical Education (AICTE) is pleased to accord approval to **Vivekananda College of Engineering & Technology, Nehru Nagar, Puttur, D.K. - 574 203** for extension of AICTE Approval / Introduction of new course(s) / Variation in intake (Increase / Decrease), as applicable, for Under Graduate degree level course(s) in **Degree Engineering** with Annual Intake for each course as given below: -

FULL TIME COURSE(S)	EXISTING ANNUAL INTAKE	REVISED APPROVED INTAKE	ENTRY LEVEL	DURATION (YEARS)	PERIOD OF APPROVAL
COMPUTER SC. & ENGINEERING	45	60	10+2	4 years	2004-05
ELECTRONICS & COMM ENGINEERING	45	60	10+2	4 years	2004-05
INFORMATION SCIENCE & ENGG.	45	60	10+2	4 years	2004-05
MECHNICAL ENGG.	60	60	10+2	4 years	2004-05
CIVIL ENGG.	60	60	10+2	4 years	2004-05
TOTAL APPROVED INTAKE	**255**	**300**			

Contd... 2/-

इंदिरा गांधी खेल परिसर, इन्द्रप्रस्थ एस्टेट, नई दिल्ली – 110002
Indira Gandhi Sports Complex, I. P. Estate, New Delhi -110 002
दूरभाष / Phone : 23392506, 63-65-68, 71, 73 -75 फैक्स / Fax : 011-23392554
वैबसाइट / Website : www.aicte.ernet.in

The Approval accorded above is subject to the conditions that any of the following is not violated or intervened during the period of validity of said approval:

1. The institution must continue to have Affiliation to a University for the above courses before making admissions. In the absence of such Affiliation this letter of approval shall be treated as Withdrawn (Order of the High Court of Madras in W. P. No. 33256 of 2002 and other Batch of Petitions).

2. The approved course(s) shall commence as per the academic calendar of the Affiliating University.

3. This approval is subject to the concerned State / UT Admission Authority's discretion to allow admission of the students for the academic year 2004-05. In case the Admission is not allowed in the current academic year 2004-05 by the State / UT Admission Authority, the above approval shall stand valid for the next academic year 2005-06.

4. No excess admission shall be made by the Institution during any academic year.

5. Any other condition(s) as may be specified by AICTE form time to time.

6. Consequent to the Supreme Court Judgment, the Model Constitution of Governing Body notified by AICTE in its approval Regulations 1994, stands overruled. It has been decided that while AICTE will not insist on any nomination in the Governing Body of Private Unaided Institutions, the Affiliating University / State Government shall impose minimum conditions of affiliation, such as, prescription of qualifications of Governing Body Members, in order to ensure academic excellence. It shall be desirable for the private unaided institutions to induct at least 50% of the members of the Governing Body drawn from renowned academia, academic administrators, Subject Experts and professionals from industry, in order to seek their innovative ideas for continuous improvement in the delivery of teaching learning process, matching best practices elsewhere and achieve excellence.

7. In exercise of power conferred under 10(p) of the AICTE Act, AICTE, may inspect the institution any time, it may deem fit to verify the progress / compliance or for any other purpose.

The suggested improvements, enclosed, herewith, should be complied with before the commencement of the next academic year, failing which appropriate action may be effected.

---------- 3

In the event of infringement / contravention or non-compliance of the above Conditions and / or the provisions of AICTE Act & Regulations / Guidelines / Norms & Standards as prescribed by AICTE, further actions leading to "Reduced Intake" or "No Admission or Withdrawal of Approval, may be taken by AICTE and the liability arising out of such action shall be solely that of the Management of the Institution.

Yours faithfully,

(Prof. R. S. Gaud)
Adviser (UG)

Encl.: Suggested Improvements (Specific Conditions) :

Copy to:

1. The Regional Officer, AICTE, South-West Regional Office, Health Centre build., Bangalore University campus Bangalore-560 009
2. The Registrar,
3. **The Principal**
   Vivekananda College of Engineering & Technology,
   Nehru Nagar, Puttur, D.K. - 574 203
   Karnataka
4. The Director of Technical Education, Govt. of Karnataka, Place Road, Bangalore-560 001
5. Guard File.

NAME AND ADDRESS OF THE INSTITUTION	PROGRAMME
Vivekananda College of Engineering & Technology Nehru Nagar, Puttur, D.K. - 574 203	Degree in Engineering

DEFICIENCIES / SUGGESTED IMPROVEMENTS::

1) 15 Journals available against the requirement of 60 , thereby resulting in a shortfall of 45 (75%)as per AICTE Norms.

2) 0 Professors are available against the requirement of 6, thereby resulting in a shortfall of 6 (100%)as per AICTE Norms.

3) 2 Asst. Professors are available against the requirement of 14, thereby resulting in a shortfall of 12 (85%)as per AICTE Norms.

4) 21 Lecturers are available against the requirement of 27 , thereby resulting in a shortfall of 6 (22%)as per AICTE Norms.

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ALL INDIA COUNCIL FOR TECHNICAL EDUCATION
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RESTORATION OF INTAKE

F.No : 770-53-296(E)/ET/2001
July 08, 2005

To
The Secretary Education Department
Govt. of Karnataka,
M.S.Building, Dr. B.R.Ambedkar Veedhi,
Bangalore-560 001, Karnataka

Sub: AICTE approval for restoration of intake for VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY,, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA for the year 2005-06-reg.

Ref: 1. Council's letter of even no. dated June 8, 2005
2. Appeal of the institution dated 25-06-05&7.7.2005.

Sir,

In continuation to the Councils earlier letter referred above, the revised intake for the year 2005-06 in respect of VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY,, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA is as under.

COURSE (S)	APPROVED INTAKE 2005-06	REVISED APPROVED INTAKE 2005-06
COMPUTER SC. & ENGINEERING	60	60
INFORMATION SCIENCE & ENGG.	**00**	**60**
ELECTRONICS & COMM ENGINEERING	60	60
MECHANICAL ENGG.	60	60
CIVIL ENGG.	60	60
TOTAL	240	300

All other terms and conditions in the letter referred above remain unchanged.

Yours faithfully

(Dr. P. Venkateswara Rao)
Adviser (UG/ PG)

Copy to :

1. The Principal,
VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY,,
NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203
KARNATAKA

2. The Regional Officer, South-West Regional Office, AICTE, Health Centre Building, Bangalore University Campus, Bangalore-560 009, Karnataka

3. The Director, Directorate of Technical Education, Govt. of Karnataka, Palace Road, Bangalore-560 001

4. The Registrar Visveswaraiah Technological University, Santibastawad Road, Machhe, Belgaum.

5. GuardFile.

11.7.05

अखिल भारतीय तकनीकी शिक्षा परिषद्
ALL INDIA COUNCIL FOR TECHNICAL EDUCATION
(भारत सरकार का एक सांविधिक निकाय) (A STATUTORY BODY OF THE GOVT. OF INDIA)

F. No. 770-53-262(E)/ET/96 **Date: 15/05/2006**

To,

The Principal Secretary,
Government of Karnataka,
Multistoried Building,
Dr. B.R. Ambedkar Veedhi,
Bangalore – 560 001

Sub: AICTE approval for extension / increase / variation in intake / introduction of additional courses to the **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOG, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST – 574 203 KARNATAKA** for the academic year 2006-07.

Sir,

As per the Regulations notified by the Council vide F.No. 37-3/Legal/2004 dated 28th November 2005 and norms, standards, procedures and conditions prescribed by the Council from time to time the compliance report / proposal for increase / variation in intake / introduction of additional courses submitted by VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOG, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST – 574 203 KARNATAKA has been processed through an Appraisal Committee / Hearing Committee and I am directed to convey the approval of the Council for the courses and intake as per the details given below:

Name of the Course(s)	Existing Intake	Revised Intake	Period of approval
CIVIL ENGG.	60	60	2006-2007
COMPUTER SCIENCE & ENGINEERING	60	60	
ELECTRONICS & COMM. ENGG.	60	60	
INFORMATION SCIENCE & ENGG.	60	60	
MECHANICAL ENGINEERING	60	60	
Total	**300**	**300**	

The above approval is subject to rectification of the following observations / deficiencies / specific conditions by 31st August 2006.

- Principal not qualified as per AICTE norms.

Contd.. 2/-

इंदिरा गांधी खेल परिसर, इन्द्रप्रस्थ एस्टेट, नई दिल्ली – 110002
Indira Gandhi Sports Complex, I. P. Estate, New Delhi-110 002
दूरभाष / Phone : 23392506, 63-65-68, 71, 73 -75 फैक्स / Fax : 011-23392554
वैबसाइट / Website : www.aicte.ernet.in

copy to the correspondence

Note: 1. The mandatory disclosure in prescribed format if not hosted on the website should be hosted by 31st May, 2006, failing which action would be initiated as per the rules and regulations of the AICTE including No Admission / Withdrawal of approval.

The institution is required to submit two copies of the Compliance Report, indicating the rectification of deficiencies along with mandatory disclosure and details of faculty recruited for each course in the prescribed format (available at AICTE Website www.aicte.ernet.in) to the concerned Regional Office latest by 31st August 2006 for consideration of approval beyond the session 2006-07.

The Compliance Report must be accompanied with a processing fee of Rs. 40,000/- in the form of demand draft in the favour of Member Secretary, AICTE, payable at New Delhi. In the absence of processing fee the Compliance Report will not be entertained. Following the Compliance report, the Council would verify the status in respect of rectification of deficiencies through surprise random inspection without any prior notice.

The above approval if granted after rectification of deficiencies would be subject to the fulfillment of the following general conditions:

1 That the management shall provide adequate funds for development of land and for providing related infrastructural, instructional and other facilities as per norms and standards laid down by the Council from time to time and for meeting recurring expenditure.

2. (a) That the admission shall be made only after adequate infrastructure and all other facilities are provided as per norms and guidelines of the AICTE.

(b) That the admissions shall be made in accordance with the regulations notified by the Council from time to time.

(c) That the curriculum of the course, the procedure for evaluation/ assessment of students shall be in accordance with the norms prescribed by the AICTE.

(d) That the Institution shall not allow closure of the Institution or discontinuation of the course(s) or start any new course(s) or alter intake capacity of seats without the prior approval of the Council.

(e) **That no excess admission shall be made by the Institution over and above the approved intake under any circumstances. In case any excess admission is reported to the Council, appropriate penal action including withdrawal of approval shall be initiated against the Institution**

(f) **That the institutions shall not have any collaborative arrangements with any Indian and/ or Foreign Universities for conduct of technical courses other than those approved by AICTE without obtaining prior approval from AICTE. In case any violation is reported to the Council, appropriate penal action including withdrawal of approval shall be initiated against the Institution.**

(g) **That the Institution shall not conduct any course(s) in the field of technical education in the same premises/ campus and / or in the name of the Institution without prior permission/ approval of AICTE. In case any violation is reported to the Council, appropriate penal action including withdrawal of approval shall be initiated against the Institution**

(h) **The institution shall not conduct any non-technical course(s) in the same premises/ campus under any circumstances. In case any violation is reported to the Council, appropriate penal action including withdrawal of approval shall be initiated against the Institution**

contd.. 3/-

3 That the institution shall operate only from the approved location, and that the institution shall not open any off campus study centers/ extension centers directly or in collaboration with any other institution/ university/ organization for the purpose of imparting technical education without obtaining prior approval from the AICTE.

4 That the tuition and other fees shall be charged as prescribed by the Competent Authority within the overall criteria prescribed by the Council from time to time. No capitation fee shall be charged from the students/ guardians of students in any form.

5 That the accounts of the Institution shall be audited annually by a certified Chartered Accountant and shall be open for inspection by the Council or any body or persons authorized by it.

6 That the Director/ Principal and the teaching and other staff shall be selected according to procedures, qualifications and experience prescribed by the Council from time to time and pay scales are as per the norms prescribed by the Council from time to time.

7 (a) That the institution shall furnish requisite returns and reports as desired by AICTE in order to ensure proper maintenance of administrative and academic standards.

(b) That the technical institution shall publish an information booklet before commencement of the academic year giving details regarding the institution and courses/ programmes being conducted and details of infrastructural facilities including faculty etc. in the form of mandatory disclosure. The information booklet may be made available to the stakeholders of the technical education on cost basis. The mandatory disclosure information shall be put on the Institution Website. The information shall be revised every year with updated information about all aspects of the institution.

(c) That it shall be mandatory for the technical institution to maintain a Website providing the prescribed information. The Website information must be continuously updated as and when changes take place.

(d) That a compliance report in the prescribed format along with mandatory disclosures on fulfillment of the above conditions, shall be submitted each year by the Institution within the time limit prescribed by the Council from time to time **i.e. 31st August 2006 for the current year.**

(e) That if Technical Institution fails to disclose the information or suppress and/ or misrepresent the information, appropriate action could be initiated including withdrawal of AICTE approval.

8 That all the laboratories, workshops etc. shall be equipped as per the syllabi of the concerned affiliated University and shall be in operational condition before making admissions.

9 That a library shall be established with adequate number of titles, books, journals (both Indian & Foreign) etc as per AICTE norms.

10 That a computer center with adequate number of terminals, Printers etc. shall be established as per AICTE norms.

11 AICTE may carry out random inspections round the year for verifying the status of the Institutions to ensure maintenance of norms and standards.

12 That the AICTE may also conduct inspections with or without notifying the dates to verify specific complaints of mis-representation, violation of norms and standards, mal-practices etc.

13 That the Institution by virtue of the approval given by Council shall not automatically become claimant to any grant-in-aid form the Central or State Government.

14 That the Management shall strictly follow further conditions as may be specified by the Council from time to time.

contd.. 4/-

14 In the event of non-compliance by the **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA** with regard to guidelines, norms and conditions prescribed from time to time the Council shall be free to take measures for withdrawal of its approval or recognition, without consideration of any related issues and that all liabilities arising out of such withdrawal would solely be that of **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA .**

Yours faithfully,

(Harish C. Rai)
Adviser- UG/PG (E&T)

Copy to:

1. The Principal,
   VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY,
   NEHRU NAGAR,
   PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203
   KARNATAKA
2. The Regional Officer, AICTE, South-West Regional Office, Bangalore University Campus P.K. Block, Palace Road, Bangalore – 560 009.
3. The Commissioner of Tech. Education, Government of Karnataka, Palace Road, Bangalore – 560 001
3. The Registrar, concerned University.
   (He is requested to complete the process of affiliation for facilitating admissions).
4. Guard File (UG/PG).

अखिल भारतीय तकनीकी शिक्षा परिषद्
ALL INDIA COUNCIL FOR TECHNICAL EDUCATION
(भारत सरकार का एक सांविधिक निकाय) (A STATUTORY BODY OF THE GOVT. OF INDIA)

Corrigendum

F.No. 770-53-296(E)/ET/2001
July 24, 2007

To,

The Principal Secretary
Govt. of Karnataka,
Multistoried Building
Dr. B. R. Ambedkar Veedhi
Bangalore-560 001

Sub : AICTE Approval for extension / increase/ Variation in intake/ introduction of additional courses to **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, P UTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA** for the year 2007-2008 – reg.

Sir,

In suppression of earlier letter of even no dated 20.07.2007 In continuation to Council's letter referred above, the revised intake for the year 2007-2008 in respect of **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA** is as under :

Name of the Course(s)	Existing Intake	Revised Intake	Period of approval
CIVIL ENGINEERING	60	60	2007-2008
COMPUTER SCIENCE & ENGINEERING	60	60	
ELECTRONICS & COMMUNICATION ENGG.	60	60	
INFORMATION SCIENCE & ENGG.	60	60	
MECHANICAL ENGINEERING	60	60	
MBA	00	60*	
TOTAL	300	360	

Note : * The approval for additional course(s) / increase in intake / variation in intake is valid for two years from the date of issue of this letter for getting affiliation with respective university and fulfilling State Government requirements of admission.

The additional intake is being granted based on the projections shown in the Detailed Project Report regarding additional built up space, faculty and other facilities for the proposed intake. It may be noted that all facilities including additional built area and appointment of faculty should be made available before the commencement of the next academic session. Random surprise inspection would be carried out to verify facilities and if the institute is found deficient in fulfillment of norms & standards of AICTE, appropriate action would be initiated by the Council.

Please note that other terms & conditions in the earlier letter of even no dated 12.05.2007 will remain unchanged.

Yours faithfully,

(Harish C. Rai)
Adviser- UG/PG (E&T)

Copy to:

1. The Principal,
VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY,
NEHRU NAGAR, PUTTUR TALUK, DAKSHINA
KANNADA DIST.-574 203
KARNATAKA

VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY 181 PUTTUR. D.K. 28/7/07

इंदिरा गांधी खेल परिसर, इन्द्रप्रस्थ एस्टेट, नई दिल्ली – 110002
Indira Gandhi Sports Complex, I. P. Estate, New Delhi-110 002
दूरभाष / Phone : 23392506, 63-65-68, 71, 73-75 फैक्स / Fax : 011-23392554
वैबसाइट / Website : www.aicte.ernet.in

2. The Regional Officer,
   AICTE Southern West Regional Office,
   Banaglore University Campus, P.K.Block,
   Palace Road, Bangalore – 560 009

3. The Director of Tech. Education
   Govt. of Karnataka,
   Palace Road, Banaglore-560 001

4. The Registrar, concerned University.
   (He is requested to complete the process of affiliation for facilitating admissions).

5. Guard File (UG/PG).

अखिल भारतीय तकनीकी शिक्षा परिषद्
ALL INDIA COUNCIL FOR TECHNICAL EDUCATION

(भारत सरकार का सांविधिक निकाय) (A statutory body of the Govt. of India)

F. No. 770-53-296(E)/ET/2001

May 2, 2008

The Principal Secretary
Govt. of Karnataka,
Multistoried Building
Dr. B. R. Ambedkar Veedhi
Bangalore-560 001

Sub: Extension of approval to VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA

Sir,

As per the Regulations notified by the Council vide F.No. 37-3/Legal/2004 dated 14th September 2006 and norms, standards, procedures and conditions prescribed by the Council from time to time and based on the recommendations of Appraisal Committee / Expert Committee, I am directed to convey the extension of approval of the Council to **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA** for conduct of the following courses with the intake indicated below:

Name of the Course (s)	Existing Intake	Revised Intake	Period of approval
CIVIL ENGINEERING	60	60	2008-10*
COMPUTER SCIENCE & ENGINEERING	60	60	
ELECTRONICS & COMMUNICATION ENGG.	60	60	
INFORMATION SCIENCE & ENGG.	60	60	
MBA	60	60	
MECHANICAL ENGG.	60	60	
Total	360	360	

*** The Compliance Report along with requisite processing fee is required to be submitted every year by August 31 irrespective of the period of approval.**

The above approval is subject to rectification of the following observations / deficiencies / specific conditions by 31st August 2008.

- **Faculty :**
  - Faculty with proper cadre ratio, requisite qualifications and experience to be appointed in all the disciplines as per AICTE norms.
  - The faculty shortfall in various branches is as follows:

Course (s)	Faculty required	Faculty available	Shortfall Number
CIVIL ENGINEERING	12	11	01
COMPUTER SCIENCE & ENGINEERING	12	11	01
INFORMATION SCIENCE & ENGG.	12	11	01
MECHANICAL ENGG.	12	11	01
H & S	20	10	10

- **COMPUTER FACILITY:**

Required	Available	Shortfall Number
330	324	06

- **LIBRARY FACILITY:**
  - Number of Titles of books/volumes/Journals to be increased as per AICTE norms.

Contd.. 2/-

Received on 19/7/2008

6 That the Director/ Principal and the teaching and other staff shall be selected according to procedures, qualifications and experience prescribed by the Council from time to time and pay scales are as per the norms prescribed by the Council from time to time.

7 (a) That the institution shall furnish requisite returns and reports as desired by AICTE in order to ensure proper maintenance of administrative and academic standards.

(b) That the technical institution shall publish an information booklet before commencement of the academic year giving details regarding the institution and courses/ programmes being conducted and details of infrastructural facilities including faculty etc. in the form of mandatory disclosure. The information booklet may be made available to the stakeholders of the technical education on cost basis. The mandatory disclosure information shall be put on the Institution Website. The information shall be revised every year with updated information about all aspects of the institution.

(c) That it shall be mandatory for the technical institution to maintain a Website providing the prescribed information. The Website information must be continuously updated as and when changes take place.

(d) That a compliance report in the prescribed format along with mandatory disclosures on fulfillment of the above conditions, shall be submitted each year by the Institution within the time limit prescribed by the Council from time to time **i.e. 31st August 2008 for the current year.**

(e) That if Technical Institution fails to disclose the information or suppress and/ or misrepresent the information, appropriate action could be initiated including withdrawal of AICTE approval.

8 That all the laboratories, workshops etc. shall be equipped as per the syllabi of the concerned affiliated University and shall be in operational condition before making admissions.

9 That a library shall be established with adequate number of titles, books, journals (both Indian & Foreign) etc as per AICTE norms.

10 That a computer center with adequate number of terminals, Printers etc. shall be established as per AICTE norms.

11 AICTE may carry out random inspections round the year for verifying the status of the Institutions to ensure maintenance of norms and standards.

12 That the AICTE may also conduct inspections with or without notifying the dates to verify specific complaints of mis-representation, violation of norms and standards, mal-practices etc.

13 That the Institution by virtue of the approval given by Council shall not automatically become claimant to any grant-in-aid form the Central or State Government.

14 That in the event of student/candidate withdrawing before the starting of the course, the wait listed candidates should be given admission against the vacant seat. The entire fee collected from the student, after a deduction of the processing fee of not more than Rs. 1000/- (Rupees one thousand only) shall be refunded and returned by the Institution/University to the student/candidate withdrawing from the programme. It would not be permissible for Institutions and Universities to retain the School/Institution Leaving Certificate in original to force retention of admitted students (See Public Notice aicte/DPG/03(01)/2008)

15 The Institute shall take appropriate measures for prevention of ragging in any form, in the light of directions of Supreme Court of India in Writ Petition No. © 656/1998. Incase of failure to prevent the instances of ragging by the Institutions, the Council shall take appropriate action including withdrawal of approval .

16 That the Management shall strictly follow further conditions as may be specified by the Council from time to time.

Note: The mandatory disclosure in prescribed format is required to be hosted on the website as per directions in the AICTE website failing which, action would be initiated as per the rules and regulations of the AICTE including No Admission / Withdrawal of approval.

The institution is required to submit two copies of the Compliance Report, indicating the rectification of deficiencies along with mandatory disclosure and details of faculty recruited for each course in the prescribed format (available at AICTE Website www.aicte.ernet.in) to the concerned Regional Office latest by 31st August 2008 for consideration of approval beyond the session 2008-09. **It may be noted that all the institutions are required to submit the compliance Report alongwith requisite processing fee by 31st August every year irrespective of the period of approval .**

The Compliance Report must be accompanied with a processing fee of Rs. 40,000/- in the form of demand draft in the favour of Member Secretary, AICTE, payable at New Delhi. In the absence of processing fee the Compliance Report will not be entertained Following the Compliance report, the Council would verify the status in respect of rectification of deficiencies through surprise random inspection without any prior notice.

The above approval if granted after rectification of deficiencies would be subject to the fulfillment of the following general conditions:

1 That the management shall provide adequate funds for development of land and for providing related infrastructural, instructional and other facilities as per norms and standards laid down by the Council from time to time and for meeting recurring expenditure.

2. (a) That the admission shall be made only after adequate infrastructure and all other facilities are provided as per norms and guidelines of the AICTE.

(b) That the admissions shall be made in accordance with the regulations notified by the Council from time to time.

(c) That the curriculum of the course, the procedure for evaluation/ assessment of students shall be in accordance with the norms prescribed by the AICTE.

(d) That the Institution shall not allow closure of the Institution or discontinuation of the course(s) or start any new course(s) or alter intake capacity of seats without the prior approval of the Council.

(e) That no excess admission shall be made by the Institution over and above the approved intake under any circumstances In case any excess admission is reported to the Council, appropriate penal action including withdrawal of approval shall be initiated against the Institution

(f) That the institutions shall not have any collaborative arrangements with any Indian and/ or Foreign Universities for conduct of technical courses other than those approved by AICTE without obtaining prior approval from AICTE. In case any violation is reported to the Council, appropriate penal action including withdrawal of approval shall be initiated against the Institution

(g) That the Institution shall not conduct any course(s) in the field of technical education in the same premises/ campus and / or in the name of the Institution without prior permission/ approval of AICTE. In case any violation is reported to the Council, appropriate penal action including withdrawal of approval shall be initiated against the Institution

(h) The institution shall not conduct any non-technical course(s) in the same premises/ campus under any circumstances. In case any violation is reported to the Council, appropriate penal action including withdrawal of approval shall be initiated against the Institution

3 That the institution shall operate only from the approved location, and that the institution shall not open any off campus study centers/ extension centers directly or in collaboration with any other institution/ university/ organization for the purpose of imparting technical education without obtaining prior approval from the AICTE.

4 That the tuition and other fees shall be charged as prescribed by the Competent Authority within the overall criteria prescribed by the Council from time to time. No capitation fee shall be charged from the students/ guardians of students in any form.

5 That the accounts of the Institution shall be audited annually by a certified Chartered Accountant and shall be open for inspection by the Council or any body or persons authorized by it.

contd.. 3/-

17. In the event of non-compliance by the **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA** with regard to guidelines, norms and conditions prescribed from time to time the Council shall be free to take measures for withdrawal of its approval or recognition, without consideration of any related issues and that all liabilities arising out of such withdrawal would solely be that of **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA**

Yours faithfully.

(Harish C. Rai)
Adviser- UG/PG (E&T)

Copy to:

1. The Principal,
   VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA
2. The Regional Officer, AICTE, South-West Regional Office, Bangalore University Campus P.K. Block, Palace Road, Bangalore – 560 009.
3. The Commissioner of Tech. Education, Government of Karnataka, Palace Road, Bangalore – 560 001
4. The Registrar, concerned University.
   (He is requested to complete the process of affiliation for facilitating admissions).
5. Guard File (UG/PG).

अखिल भारतीय तकनीकी शिक्षा परिषद्
ALL INDIA COUNCIL FOR TECHNICAL EDUCATION

(भारत सरकार का एक सांविधिक निकाए) (A STATUTORY BODY OF THE GOVT. OF INDIA)

Revised Letter (Increase in intake)

F.No. 770-53-296(E)/ET/2001
Dt. June 26, 2009

To,

The Principal Secretary, (Tech. Education)
Government of Karnataka,
Multistoried Building,
Dr. B.R. Ambedkar Veedhi,
Bangalore – 560 001
Ph:- 080-28432837/ 28432106
Fax-080-28432837

Sub : AICTE Approval for extension / increase/ Variation in intake/ introduction of additional courses to **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA** for the year 2009-2010 – reg.

Sir,

In continuation to Council's earlier extension of approval letter the revised intake for the year 2009-2010 in respect of **VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY, NEHRU NAGAR, PUTTUR TALUK, DAKSHINA KANNADA DIST.-574 203 KARNATAKA** is as under:

Name of the Course(s)	Existing Intake	Revised Intake
CIVIL ENGINEERING	60	**120***
COMPUTER SCIENCE & ENGINEERING	60	**90***
ELECTRONICS & COMMUNICATION ENGG.	60	60
INFORMATION SCIENCE & ENGG.	60	60
MECHANICAL ENGG.	60	**90***
MBA	60	60
Total --→	**360**	**480**

Note : * The approval for additional course(s) / increase in intake / variation in intake is valid for two years from the date of issue of this letter for getting affiliation with respective university and fulfilling State Government requirements of admission.

The additional intake is being granted based on the projections shown in the Detailed Project Report regarding additional built up space, faculty and other facilities for the proposed intake. It may be noted that all facilities including additional built area and appointment of faculty should be made available before the commencement of the next academic session. Random surprise inspection would be carried out to verify facilities and if the institute is found deficient in fulfillment of norms & standards of AICTE, appropriate action would be initiated by the Council.

Please note that other terms & conditions in the earlier extension of approval letter will remain unchanged.

Yours faithfully,

(DevVrat Singh)
Adviser- (E&T)

Copy to:

1. THE PRINCIPAL/DIRECTOR
VIVEKANANDA COLLEGE OF ENGINEERING & TECHNOLOGY,
NEHRU NAGAR, PUTTUR TALUK, DAKSHINA
KANNADA DIST.-574 203 KARNATAKA

2. The Regional officer,
AICTE Southern West Regional Office,
Banaglore University Campus, P.K.Block,
Palace Road, Bangalore – 560 009

3. The Commissioner of Tech. Education,
Government of Karnataka,
Palace Road, Bangalore – 560 001

4. The Registrar
Visweswaraiah Technology University,
Machechе Campus, Santebatawad Road,
Belgaum-580 014

5. **Guard File (E&T)**

404

All India Council for Technical Education
(A Statutory Body under Ministry of HRD,Govt of India)
7th floor, Chandralok Building, Janpath, New Delhi 110 001
Phone : 11 23724151-57 FAX : 11 23724183 www.aicte-india.org

No. : South-West Region/1-2145671/2010/EOA **August 23, 2010**

To,
Principal Secretary (Hr. & Tech Education) Govt. of Karnataka, K. G.S.,
6th Floor, M.S. Building, R. N. 645, Dr. B. R. Ambedkar Road,

Sub. : Extension of approval for the academic year 2010-11.

Sir,

In terms of the Regulations notified by the Council vide F. No. 37-3/Legal/2010 and norms, standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the extension of approval of the Council to :

VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR, VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY, NEHARU NAGARAPUTTUR TALUKDAKSHINA KANNADAKARNATAKA574203, PUTTUR, KARNATAKA, PIN : 574203

for conduct of the following courses with the intake indicated below in the academic year 2010-11:

Sr. No.	Program	Level	Shift	Course	Intake 2009-10	Intake 2010-11
1	Engg. / Tech.	UG	First Shift	MECHANICAL ENGINEERING	90	90
2	Engg. / Tech.	UG	First Shift	INFORMATION TECHNOLOGY	60	60
3	Engg. / Tech.	UG	First Shift	ELECTRICAL & COMMUNICATION	60	60
4	Engg. / Tech.	UG	First Shift	COMPUTER SCIENCE & ENGINEERING	90	90
5	Engg. / Tech.	UG	First Shift	CIVIL ENGINEERING	120	120
6	Engg. / Tech.	PG	First Shift	MBA	60	60

The above mentioned approval is subject to the condition that :

VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR, VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY, NEHARU NAGARAPUTTUR TALUKDAKSHINA KANNADAKARNATAKA574203, PUTTUR, KARNATAKA, PIN : 574203

shall follow and adhere to the regulations, guidelines and directions issued by AICTE from time to time and the undertaking / affidavit given by the institution along with the application submitted by the institution on portal and hard copy to Regional Office.

Anti Ragging :- The approval is subject to the institutions strictly complying with all the provisions made under the Anti ragging regulation notified by council vide F.No. 37/Legal/AICTE/2009 dated 1-7-2009 failing which, it will be liable to any action defined under clause 9(4) of this regulation.

Yours faithfully,

Dr. S. G. Bhirud
Director

South Western Regional Office
All India Council for Technical Education
Bangalore-9

All India Council for Technical Education
(A Statutory Body under Ministry of HRD,Govt of India)

7th floor, Chandralok Building, Janpath, New Delhi 110 001
Phone : 11 23724151-57 FAX : 11 23724183 www.aicte-india.org

Copy to :

1. The Regional Office, South-West Region, Karnataka
2. The Director of Technical Education, Govt. of Delhi.
3. Guard File (AICTE)
4. The Registrar, Affiliating University
5. The Principal / Director,
   VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR, VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY, NEHARU NAGARAPUTTUR TALUKDAKSHINA KANNADAKARNATAKA574203, PUTTUR, KARNATAKA, PIN : 574203

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

F.No. South-West/1-403108932/2011/EOA Date: 01-09-2011

To,
The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of approval for the academic year 2011-12.
Ref : Application of the Institution for Extension of Approval for the Year 2011-12

Sir/Madam,

In terms of the Regulations notified by the Council vide F.No. 37-3/Legal/2011 dated 10/12/2010 and norms, standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the extension of approval of the Council to

Regional Office	South-West	Application Id	1-403108932
		Permanent Id	1-2145671
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203,PUTTUR,DAKSHINA KANNADA,Karnataka,574203
Name of the Society/Trust	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)	Society/Trust Address	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institute Type	Unaided - Private		

to conduct following courses with the intake indicated below for the academic year 2011-12

Application Id: 1-403108932			Course	Full/Part Time	Affiliating Body	Intake 2010-11	Intake Approved for 11-12	NRI	PIO	Foreign Collaboration
Program	Shift	Level								
MANAGEMENT	1st Shift	POST GRADUATE	MASTERS IN BUSINESS ADMINISTRATION	FULL TIME	Visvesvaraya Technological University, Belagaum	60	60	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	MECHANICAL ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belagaum	90	120	No	No	No

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Date of printing: 02-09-2011

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

Application Id: 1-403108932			Course	Full/Part Time	Affiliating Body	Intake 2010-11	Intake Approved for 11-12	NRI	PIO	Foreign Collaboration
Program	Shift	Level								
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	CIVIL ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belagaum	120	120	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belagaum	60	60	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	INFORMATION SCIENCE AND ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belagaum	60	60	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belagaum	90	90	No	No	No

The above mentioned approval is subject to the condition that VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY shall follow and adhere to the Regulations, guidelines and directions issued by AICTE from time to time and the undertaking / affidavit given by the institution along with the application submitted by the institution on portal.

In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Strict compliance of Anti-Ragging Regulation:- Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 37-3/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

(Dr. K P Isaac)

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Date of printing: 02-09-2011

Member Secretary, AICTE

Copy to:

1. **The Regional Officer,**
   All India Council for Technical Education
   Health Centre Building
   Bangalore University Campus
   Bangalore - 560 009, Karnataka

2. **The Director Of Technical Education,**
   Karnataka

3. **The Registrar,**
   Visvesvaraya Technological University, Belagaum

4. **The Principal / Director,**
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
   NEHARU NAGARA
   PUTTUR TALUK
   DAKSHINA KANNADA
   KARNATAKA
   574203,
   PUTTUR,DAKSHINA KANNADA,
   Karnataka,574203

5. **The Secretary / Chairman,**
   VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
   VIVEKANANDA COLLEGE CAMPUS
   NEHARU NAGARA,
   PUTTUR,D KANNADA(DK),
   Karnataka,574203

6. **Guard File(AICTE)**

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Date of printing: 02-09-2011

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

F.No. South-West/1-687532801/2012/EOA

Date: 10 May 2012

To,
The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of approval for the academic year 2012-13

Ref: Application of the Institution for Extension of approval for the academic year 2012-13

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations 2010 notified by the Council vide notification number F-No.37-3/Legal/2010 dated 10/12/2010 and amendment vide notification number F-No.37-3/Legal/2011 dated 30/09/2011 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Regional Office	South-West	Application Id	1-687532801
		Permanent Id	1-2145671
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203
Name of the Society/Trust	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)	Society/Trust Address	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institute Type	Unaided - Private		

Opted for change from Women to Co-ed	No	Opted for change of name	No	Opted for change of site	No
Change from Women to Co-ed approved	Not Applicable	Change of name Approved	Not Applicable	Change of site Approved	Not Applicable

to conduct following courses with the intake indicated below for the academic year 2012-13

Note: This is a Computer generated Extension of Approval Letter. No signature is required.

Letter Printed On:17 May 2012.

Printed By : AE133141

Application Id: 1-687532801			Course	Full/Part Time	Affiliating Body	Intake 2011-12	Intake Approved for 12-13	NRI	PIO	Foreign Collaboration
Program	Shift	Level								
MANAGEMENT	1st Shift	POST GRADUATE	MASTERS IN BUSINESS ADMINISTRATION	FULL TIME	Visvesvaraya Technological University, Belagaum	60	60	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	MECHANICAL ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belagaum	120	120	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	CIVIL ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belagaum	120	120	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belagaum	60	60	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	INFORMATION SCIENCE AND ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belagaum	60	60	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belagaum	90	90	No	No	No

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Letter Printed On:17 May 2012.

Printed By : AE133141

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

Application Id: 1-687532801			Course	Full/Part Time	Affiliating Body	Intake 2011-12	Intake Approved for 12-13	NRI	PIO	Foreign Collaboration
Program	Shift	Level								
ENGINEERING AND TECHNOLOGY	1st Shift	POST GRADUATE	MACHINE DESIGN	FULL TIME	Visvesvaraya Technological University, Belagaum	0	0	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	POST GRADUATE	DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS	FULL TIME	Visvesvaraya Technological University, Belagaum	0	0	No	No	No

The above mentioned approval is subject to the condition that VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY shall follow and adhere to the Regulations, guidelines and directions issued by AICTE from time to time and the undertaking / affidavit given by the institution along with the application submitted by the institution on portal.

In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Strict compliance of Anti-Ragging Regulation:- Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 37-3/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

(Dr. K P Isaac)

Member Secretary, AICTE

Copy to:

1. **The Regional Officer,**
   All India Council for Technical Education
   Health Centre Building
   Bangalore University Campus
   Bangalore - 560 009, Karnataka

2. **The Director Of Technical Education,**
   Karnataka

3. **The Registrar,**

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Letter Printed On:17 May 2012.

Printed By : AE133141

Visvesvaraya Technological University, Belagaum

4. **The Principal / Director,**
VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
NEHARU NAGARA
PUTTUR TALUK
DAKSHINA KANNADA
KARNATAKA
574203,
PUTTUR,DAKSHINA KANNADA,
Karnataka,574203

5. **The Secretary / Chairman,**
VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
VIVEKANANDA COLLEGE CAMPUS
NEHARU NAGARA,
PUTTUR,D KANNADA(DK),
Karnataka,574203

6. **Guard File(AICTE)**

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Letter Printed On:17 May 2012.

Printed By : AE133141

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

F.No. South-West/1-1351760552/2013/EOA Date: 19-Mar-2013

To,
The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of approval for the academic year 2013-14

Ref: Application of the Institution for Extension of approval for the academic year 2013-14

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations 2012 notified by the Council vide notification number F-No.37-3/Legal/2012 dated 27/09/2012 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Regional Office	South-West	Application Id	1-1351760552
		Permanent Id	1-2145671
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203
Name of the Society/Trust	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)	Society/Trust Address	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institute Type	Unaided - Private		

Opted for change from Women to Co-ed	No	Opted for change of name	No	Opted for change of site	No
Change from Women to Co-ed approved	Not Applicable	Change of name Approved	Not Applicable	Change of site Approved	Not Applicable

to conduct following courses with the intake indicated below for the academic year 2013-14

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Letter Printed On:20 March 2013.

Printed By : ae133141

Application Id: 1-1351760552			Course	Full/Part Time	Affiliating Body	Intake 2012-13	Intake Approved for 13-14	NRI	PIO	Foreign Collaboration
Program	Shift	Level								
ENGINEERING AND TECHNOLOGY	1st Shift	POST GRADUATE	COMPUTER INTEGRATED MANUFACTURING	FULL TIME	Vesveswaraiah Technological University, Belgaum	0	18	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	POST GRADUATE	DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS	FULL TIME	Vesveswaraiah Technological University, Belgaum	0	18	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	CIVIL ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	90	120	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	60	120	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	INFORMATION SCIENCE AND ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	60	60	No	No	No
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	MECHANICAL ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	No	No	No
MANAGEMENT	1st Shift	POST GRADUATE	MASTERS IN BUSINESS ADMINISTRATION	FULL TIME	Vesveswaraiah Technological University, Belgaum	60	60	No	No	No

- Validity of the course details may be verified at www.aicte-india.org>departments>approvals

The above mentioned approval is subject to the condition that VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY shall follow and adhere to the Regulations, guidelines and directions issued by AICTE from time to time and the undertaking / affidavit

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Letter Printed On:20 March 2013.

Printed By : ae133141

given by the institution along with the application submitted by the institution on portal.

In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Strict compliance of Anti-Ragging Regulation:- Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 37-3/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

(Dr. Kuncheria P. Isaac)

Member Secretary, AICTE

Copy to:

1. **The Regional Officer,**
   All India Council for Technical Education
   Health Centre Building
   Bangalore University Campus
   Bangalore - 560 009, Karnataka

2. **The Director Of Technical Education,**
   Karnataka

3. **The Registrar,**
   Vesveswaraiah Technological University, Belgaum

4. **The Principal / Director,**
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
   NEHARU NAGARA
   PUTTUR TALUK
   DAKSHINA KANNADA
   KARNATAKA
   574203,
   PUTTUR,DAKSHINA KANNADA,
   Karnataka,574203

5. **The Secretary / Chairman,**
   VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
   VIVEKANANDA COLLEGE CAMPUS
   NEHARU NAGARA,
   PUTTUR,D KANNADA(DK),
   Karnataka,574203

6. **Guard File(AICTE)**

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Letter Printed On:20 March 2013.

Printed By : ae133141

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

F.No. South-West/1-2018909157/2014/EOA Date: 04-Jun-2014

To,
The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of approval for the academic year 2014-15

Ref: Application of the Institution for Extension of approval for the academic year 2014-15

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations 2012 notified by the Council vide notification number F-No.37-3/Legal/2012 dated 27/09/2012 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Regional Office	South-West	Application Id	1-2018909157
		Permanent Id	1-2145671
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203
Name of the Society/Trust	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)	Society/Trust Address	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institute Type	Unaided - Private		

Opted for change from Women to Co-ed	No	Opted for change of name	No	Opted for change of site	No
Change from Women to Co-ed approved	Not Applicable	Change of name Approved	Not Applicable	Change of site Approved	Not Applicable

to conduct following courses with the intake indicated below for the academic year 2014-15

Note: This is a Computer generated Letter of Approval.No signature is required. Letter Printed On:5 June 2014

Printed By : ae133141

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

Application Id: 1-2018909157			Course	Full/Part Time	Affiliating Body	Intake 2013-14	Intake Approved for 14-15	NRI Approval status	PIO Approval status	Foreign Collaboration Approval status
Program	Shift	Level								
ENGINEERING AND TECHNOLOGY	1st Shift	POST GRADUATE	COMPUTER INTEGRATED MANUFACTURING	FULL TIME	Vesveswaraiah Technological University, Belgaum	18	18	No	No	N
ENGINEERING AND TECHNOLOGY	1st Shift	POST GRADUATE	DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS	FULL TIME	Vesveswaraiah Technological University, Belgaum	18	18	No	No	N
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	CIVIL ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	No	No	N
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	No	No	N
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	ELECTRONICS AND COMMUNICATION S ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	No	No	N
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	INFORMATION SCIENCE AND ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	60	60	No	No	N
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	MECHANICAL ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	No	No	N
MANAGEMENT	1st Shift	POST GRADUATE	MASTERS IN BUSINESS ADMINISTRATION	FULL TIME	Vesveswaraiah Technological University, Belgaum	60	60	No	No	N

- Validity of the course details may be verified at www.aicte-india.org>departments>approvals

Note: This is a Computer generated Letter of Approval.No signature is required. Letter Printed On:5 June 2014

Printed By : ae133141

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

The above mentioned approval is subject to the condition that VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY shall follow and adhere to the Regulations, guidelines and directions issued by AICTE from time to time and the undertaking / affidavit given by the institution along with the application submitted by the institution on portal and subsequently upload and update the student/ faculty/ other data on portal as per the time schedule which will be intimated by AICTE.

In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Strict compliance of Anti-Ragging Regulation:- Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 37-3/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

(Dr. Kuncheria P. Isaac)

Member Secretary, AICTE

Copy to:

1. **The Regional Officer,**
   All India Council for Technical Education
   Health Centre Building
   Bangalore University Campus
   Bangalore - 560 009, Karnataka

2. **The Director Of Technical Education,**
   Karnataka

3. **The Registrar,**
   Visvesvaraya Technological University, Belagaum

4. **The Principal / Director,**
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
   NEHARU NAGARA
   PUTTUR TALUK
   DAKSHINA KANNADA
   KARNATAKA
   574203,
   PUTTUR,DAKSHINA KANNADA,
   Karnataka,574203

5. **The Secretary / Chairman,**
   VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
   VIVEKANANDA COLLEGE CAMPUS
   NEHARU NAGARA,

Note: This is a Computer generated Letter of Approval.No signature is required. Letter Printed On:5 June 2014

Printed By : ae133141

PUTTUR,D KANNADA(DK),
Karnataka,574203

6. **Guard File(AICTE)**

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

F.No. South-West/1-2456104428/2015/EOA Date: 07-Apr-2015

To,
The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of approval for the academic year 2015-16

Ref: Application of the Institution for Extension of approval for the academic year 2015-16

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations 2012 notified by the Council vide notification number F-No.37-3/Legal/2012 dated 27/09/2012 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Regional Office	South-West	Application Id	1-2456104428
		Permanent Id	1-2145671
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203
Name of the Society/Trust	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)	Society/Trust Address	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institute Type	Unaided - Private		

Opted for change from Women to Co-ed	No	Opted for change of name	No	Opted for change of site	No
Change from Women to Co-ed approved	Not Applicable	Change of name Approved	Not Applicable	Change of site Approved	Not Applicable

To conduct following courses with the intake indicated below for the academic year 2015-16

Note: This is a Computer generated Letter of Approval.No signature is required. Letter Printed On:15 April 2015

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All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

Application Id: 1-2456104428			Course	Full/Part Time	Affiliating Body	Intake 2014-15	Intake Approved for 15-16	NRI Approval status	PIO Approval status	Foreign Collaboration Approval status
Program	Shift	Level								
ENGINEERING AND TECHNOLOGY	1st Shift	POST GRADUATE	COMPUTER INTEGRATED MANUFACTURING	FULL TIME	Vesveswaraiah Technological University, Belgaum	18	18	No	No	NA
ENGINEERING AND TECHNOLOGY	1st Shift	POST GRADUATE	DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS	FULL TIME	Vesveswaraiah Technological University, Belgaum	18	18	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	CIVIL ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	INFORMATION SCIENCE AND ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	60	60	No	No	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	MECHANICAL ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	NA	NA	NA
MANAGEMENT	1st Shift	POST GRADUATE	MASTERS IN BUSINESS ADMINISTRATION	FULL TIME	Vesveswaraiah Technological University, Belgaum	60	60	NA	NA	NA

Note: Validity of the course details may be verified at www.aicte-india.org>departments>approvals

Note: This is a Computer generated Letter of Approval.No signature is required. Letter Printed On:15 April 2015

Printed By : AE133141

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

The above mentioned approval is subject to the condition that VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY shall follow and adhere to the Regulations, guidelines and directions issued by AICTE from time to time and the undertaking / affidavit given by the institution along with the application submitted by the institution on portal.

In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Strict compliance of Anti-Ragging Regulation:- Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 37-3/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

Dr. Avinash S Pant
Actg Chairman, AICTE

Copy to:

1. **The Regional Officer,**
   All India Council for Technical Education
   Health Centre Building
   Bangalore University Campus
   Bangalore - 560 009, Karnataka

2. **The Director Of Technical Education,**
   Karnataka

3. **The Registrar,**
   Vesveswaraiah Technological University, Belgaum

4. **The Principal / Director,**
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
   NEHARU NAGARA
   PUTTUR TALUK
   DAKSHINA KANNADA
   KARNATAKA
   574203,
   PUTTUR,DAKSHINA KANNADA,
   Karnataka,574203

5. **The Secretary / Chairman,**
   VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
   VIVEKANANDA COLLEGE CAMPUS
   NEHARU NAGARA,
   PUTTUR,D KANNADA(DK),
   Karnataka,574203

6. **Guard File(AICTE)**

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

F.No. South-West/1-2456104428/2015/EOA/Corrigendum-1 Date: 31-Jul-2015

Corrigendum

To,
The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of approval for the academic year 2015-16.

Ref : Application of the Institution for Extension of Approval for the Year 2015-16

EOA Issued on	F.No. South-West/1-2456104428/2015/EOA	07-Apr-2015
EOA Printed on	F.No. South-West/1-2456104428/2015/EOA	14-Jul-2015
Corrigendum 1	F.No. South-West/1-2456104428/2015/EOA/Corrigendu	31-Jul-2015

Sir/Madam,

In partial modification of the letter F.No. South-West/1-2456104428/2015/EOA and in terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations 2012 notified by the Council vide notification number F-No.37-3/Legal/2012 dated 27/09/2012 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Regional Office	South-West	Application Id	1-2456104428
		Permanent Id	1-2145671
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203,PUTTUR,DAKSHINA KANNADA,Karnataka,574203
Name of the Society/Trust	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)	Society/Trust Address	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institute Type	Unaided - Private		

Opted for change from Women to Co-ed	No	Opted for change of name	No	Opted for change of site	No
Change from Women to Co-ed approved	Not Applicable	Change of name Approved	Not Applicable	Change of site Approved	Not Applicable

To conduct following courses with the intake indicated below for the academic year 2015-16

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Letter Printed On:7 August 2015.

Printed By : ae133141

Application Id: 1-2456104428			Course	Course Unique Id	Full/Part Time	Affiliating Body	Intake Approved for 2013-14	Intake Approved for 2014-15	Intake Approved for 2015-16	NRI Approval Status	PIO Approval Status	Foreign Collaboration Approval Status
Program	Shift	Level										
MANAGEMENT	1st Shift	POST GRADUATE	MASTERS IN BUSINESS ADMINISTRATION	1-1351760878	FULL TIME	Vesveswaraiah Technological University, Belgaum	60	60	60	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	MECHANICAL ENGINEERING	1-1351760881	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	CIVIL ENGINEERING	1-1351760883	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	1-1351760885	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	1-1351760889	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	120	NA	NA	NA

Note: This is a Computer generated Extension of Approval Letter. No signature is required.
Printed By : ae133141

Letter Printed On:7 August 2015.

Application Id: 1-2456104428			Course	Course Unique Id	Full/Part Time	Affiliating Body	Intake Approved for 2013-14	Intake Approved for 2014-15	Intake Approved for 2015-16	NRI Approval Status	PIO Approval Status	Foreign Collaboration Approval Status
Program	Shift	Level										
ENGINEERING AND TECHNOLOGY	1st Shift	POST GRADUATE	DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS	1-1476379625	FULL TIME	Vesveswaraiah Technological University, Belgaum	18	18	18	NA	NA	NA

- Validity of the course details may be verified at www.aicte-india.org>departments>approvals

The above mentioned approval is subject to the condition that VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY shall follow and adhere to the Regulations, guidelines and directions issued by AICTE from time to time and the undertaking / affidavit given by the institution along with the application submitted by the institution on portal.

In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Strict compliance of Anti-Ragging Regulation:- Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 37-3/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

Dr. Avinash S Pant
Actg. Chairman, AICTE

Copy to:

1. **The Regional Officer,**
   All India Council for Technical Education
   Health Centre Building
   Bangalore University Campus
   Bangalore - 560 009, Karnataka

2. **The Director Of Technical Education,**
   Karnataka

3. **The Principal / Director,**
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
   NEHARU NAGARA
   PUTTUR TALUK
   DAKSHINA KANNADA
   KARNATAKA
   574203,

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Letter Printed On:7 August 2015.
Printed By : ae133141

PUTTUR,DAKSHINA KANNADA,
Karnataka,574203

4. **The Secretary / Chairman,**
VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
VIVEKANANDA COLLEGE CAMPUS
NEHARU NAGARA,
PUTTUR,D KANNADA(DK),
Karnataka,574203

5. **Guard File(AICTE)**

Note: This is a Computer generated Extension of Approval Letter. No signature is required. Letter Printed On:7 August 2015.
Printed By : ae133141

All India Council for Technical Education
(A Statutory body under Ministry of HRD, Govt. of India)

7th Floor, Chandralok Building, Janpath, New Delhi- 110 001
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

F.No. South-West/1-2812368994/2016/EOA Date: 05-Apr-2016

To,

The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of approval for the academic year 2016-17

Ref: Application of the Institution for Extension of approval for the academic year 2016-17

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations 2012 notified by the Council vide notification number F-No.37-3/Legal/2012 dated 27/09/2012 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Regional Office	South-West	Application Id	1-2812368994
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	Permanent Id	1-2145671
Name of the Society/Trust	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)	Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203
Institute Type	Unaided - Private	Society/Trust Address	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203

Opted for change from Women to Co-ed and Vice versa	No	Opted for change of name	No	Opted for change of site	No
Change from Women to Co-ed approved and Vice versa	Not Applicable	Change of name Approved	Not Applicable	Change of site Approved	Not Applicable

To conduct following courses with the intake indicated below for the academic year 2016-17

Application Id: 1-2812368994			Course	Full/Part Time	Affiliating Body	Intake 2015-16	Intake Approved for 2016-17	NRI Approval status	PIO / FN / Gulf quota Approval status	Foreign Collaborarion/Twining Program Approval status*
Program	Shift	Level								
ENGINEERIN	1st Shift	POST	DIGITAL ELECTRONICS	FULL TIME	Vesveswaraiah Technological	18	18	NA	NA	NA

G AND TECHNOLOGY		GRADUATE	AND COMMUNICATION SYSTEMS		University, Belgaum					
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	CIVIL ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	MECHANICAL ENGINEERING	FULL TIME	Vesveswaraiah Technological University, Belgaum	120	120	NA	NA	NA
MANAGEMENT	1st Shift	POST GRADUATE	MASTERS IN BUSINESS ADMINISTRATION	FULL TIME	Vesveswaraiah Technological University, Belgaum	60	60	NA	NA	NA

The above mentioned approval is subject to the condition that VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY shall follow and adhere to the Regulations, guidelines and directions issued by AICTE from time to time and the undertaking / affidavit given by the institution along with the application submitted by the institution on portal.

In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Strict compliance of Anti-Ragging Regulation:- Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 37-3/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

Note: Validity of the course details may be verified at www.aicte-india.org

Dr. Avinash S Pant
Vice - Chairman, AICTE

Copy to:

1. **The Regional Officer,**
   All India Council for Technical Education
   Health Centre Building
   Bangalore University Campus
   Bangalore - 560 009, Karnataka

2. **The Director Of Technical Education,**
   Karnataka

3. **The Registrar,**
   Vesveswaraiah Technological University, Belgaum

4. **The Principal / Director,**
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
   NEHARU NAGARA
   PUTTUR TALUK
   DAKSHINA KANNADA
   KARNATAKA
   574203,
   PUTTUR,DAKSHINA KANNADA,
   Karnataka,574203

5. **The Secretary / Chairman,**
   VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
   VIVEKANANDA COLLEGE CAMPUS
   NEHARU NAGARA,
   PUTTUR,D KANNADA(DK),
   Karnataka,574203

6. **Guard File(AICTE)**

All India Council for Technical Education

(A Statutory body under Ministry of HRD, Govt. of India)

Nelson Mandela MargVasant Kunj, New Delhi-110067
PHONE: 23724151/52/53/54/55/56/57 FAX: 011-23724183 www.aicte-India.org

F.No. South-West/1-3327132866/2017/EOA Date: 30-Mar-2017

To,

The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of approval for the academic year 2017-18

Ref: Application of the Institution for Extension of approval for the academic year 2017-18

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations 2016 notified by the Council vide notification number F.No.AB/AICTE/REG/2016 dated 30/11/2016 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Permanent Id	1-2145671	Application Id	1-3327132866
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203
Name of the Society/Trust	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)	Society/Trust Address	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institute Type	Unaided - Private	Region	South-West

Opted for change from Women to Co-ed and Vice versa	No	Opted for change of name	No	Opted for change of site	No
Change from Women to Co-ed approved and Vice versa	Not Applicable	Change of name Approved	Not Applicable	Change of site Approved	Not Applicable
Opted for Conversion from degree to diploma	No	Opted for Conversion from diploma to degree	No	Conversion (degree to diploma or vice-a-versa) Approved	Not Applicable

To conduct following courses with the intake indicated below for the academic year 2017-18

Application Id: 1-3327132866			Course	Full/Part Time	Affiliating Body	Intake Approved for 2016-17	Intake Approved for 2017-18	NRI Approval status	PIO / FN / Gulf quota/ OCI/ Approval status	Foreign Collaborarion/Twining Program Approval status*
Program	Shift	Level								
ENGINEERING AND	1st Shift	POST GRA	DIGITAL ELECTRONICS AND	FULL TIME	Visvesvaraya Technological University,	18	18	NA	NA	NA

TECHNOLOGY		DUATE	COMMUNICATION SYSTEMS		Belgaum					
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	CIVIL ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belgaum	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belgaum	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belgaum	120	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st Shift	UNDER GRADUATE	MECHANICAL ENGINEERING	FULL TIME	Visvesvaraya Technological University, Belgaum	120	120	NA	NA	NA
MANAGEMENT	1st Shift	POST GRADUATE	MASTERS IN BUSINESS ADMINISTRATION	FULL TIME	Visvesvaraya Technological University, Belgaum	60	60	NA	NA	NA

The above mentioned approval is subject to the condition that
VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
shall follow and adhere to the Regulations, guidelines and directions issued by AICTE from time to time and the undertaking / affidavit given by the institution along with the application submitted by the institution on portal.

In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Strict compliance of Anti-Ragging Regulation:- Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 37-3/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

Note: Validity of the course details may be verified at www.aicte-india.org

Prof. A.P Mittal
Member Secretary, AICTE

Copy to:

1. **The Regional Officer,**
   All India Council for Technical Education
   Health Centre Building
   Bangalore University Campus
   Bangalore - 560 009, Karnataka

2. **The Director Of Technical Education**,**
   Karnataka

3. **The Registrar**,**
   Visvesvaraya Technological University, Belgaum

4. **The Principal / Director,**
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
   NEHARU NAGARA
   PUTTUR TALUK
   DAKSHINA KANNADA
   KARNATAKA
   574203,
   PUTTUR,DAKSHINA KANNADA,
   Karnataka,574203

5. **The Secretary / Chairman,**
   VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
   VIVEKANANDA COLLEGE CAMPUS
   NEHARU NAGARA,
   PUTTUR,D KANNADA(DK),
   Karnataka,574203

6. **Guard File(AICTE)**

Note: ** - Approval letter copy will not be communicated through post/email. However, provision is made in the portal for downloading Approval letter through Authorized login credentials allotted to concerned DTE/Registrar.

All India Council for Technical Education

(A Statutory body under Ministry of HRD, Govt. of India)

Nelson Mandela Marg,Vasant Kunj, New Delhi-110070 Website: www.aicte-india.org

APPROVAL PROCESS 2018-19

Extension of Approval (EoA)

F.No. South-West/1-3514782706/2018/EOA Date: 04-Apr-2018

To,

The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of Approval for the Academic Year 2018-19

Ref: Application of the Institution for Extension of approval for the Academic Year 2018-19

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations 2016 notified by the Council vide notification number F.No.AB/AICTE/REG/2016 dated 30/11/2016 and amended on December 5, 2017 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Permanent Id	1-2145671	**Application Id**	1-3514782706
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	**Name of the Society/Trust**	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203	**Society/Trust Address**	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institute Type	Unaided - Private	**Region**	South-West

Opted for Change from Women to Co-Ed and vice versa	No	**Change from Women to Co-Ed and vice versa Approved or Not**	NA
Opted for Change of Name	No	**Change of Name Approved or Not**	NA
Opted for Change of Site	No	**Change of Site Approved or Not**	NA
Opted for Conversion from Degree to Diploma or vice versa	No	**Conversion for Degree to Diploma or vice versa Approved or Not**	NA
Opted for Organization Name Change	No	**Change of Organization Name Approved or Not**	NA

To conduct following Courses with the Intake indicated below for the Academic Year 2018-19

Program	Shift	Level	Course	FT/PT+	Affiliating Body (Univ/Body)	Intake Approved for 2018-19	NRI Approval Status	PIO / FN / Gulf quota/ OCI/ Approval Status	Foreign Collaboration /Twining Program Approval Status*
MANAGEMENT	1st	POST GRADUATE	MASTERS IN BUSINESS ADMINISTRATION	FT	Visvesvaraya Technological University, Belgaum	60	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st	UNDER GRADUATE	MECHANICAL ENGINEERING	FT	Visvesvaraya Technological University, Belgaum	120	NA	NA	NA
ENGINEERING AND	1st	UNDER GRADUATE	CIVIL ENGINEERING	FT	Visvesvaraya Technological University, Belgaum	120	NA	NA	NA

TECHNOLOGY									
ENGINEERING AND TECHNOLOGY	1st	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	FT	Visvesvaraya Technological University, Belgaum	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	FT	Visvesvaraya Technological University, Belgaum	120	NA	NA	NA
ENGINEERING AND TECHNOLOGY	1st	POST GRADUATE	DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS	FT	Visvesvaraya Technological University, Belgaum	18	NA	NA	NA

+FT –Full Time,PT-Part Time

In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Strict compliance of Anti-Ragging Regulation: - Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 37-3/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

Prof. A.P Mittal
Member Secretary, AICTE

Copy to:

1. The Regional Officer,
   All India Council for Technical Education
   Health Centre Building
   Bangalore University Campus
   Bangalore - 560 009, Karnataka
2. The Director Of Technical Education**,
   Karnataka
3. The Registrar**,
   Visvesvaraya Technological University, Belgaum
4. The Principal / Director,
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
   NEHARU NAGARA
   PUTTUR TALUK
   DAKSHINA KANNADA
   KARNATAKA
   574203,
   PUTTUR,DAKSHINA KANNADA,
   Karnataka,574203
5. The Secretary / Chairman,
   VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
   VIVEKANANDA COLLEGE CAMPUS
   NEHARU NAGARA,
   PUTTUR,D KANNADA(DK),
   Karnataka,574203
6. Guard File(AICTE)

Note: Validity of the Course details may be verified at http://www.aicte-india.org/

****** Individual Approval letter copy will not be communicated through Post/Email. However, consolidated list of Approved Institutions(bulk) will be shared through official Email Address to the concerned Authorities mentioned above.

All India Council for Technical Education

(A Statutory body under Ministry of HRD, Govt. of India)

Nelson Mandela Marg,Vasant Kunj, New Delhi-110070 Website: www.aicte-india.org

APPROVAL PROCESS 2019-20

Extension of Approval (EoA)

F.No. South-West/1-4261715485/2019/EOA Date: 30-Apr-2019

To,

The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of Approval for the Academic Year 2019-20

Ref: Application of the Institution for Extension of approval for the Academic Year 2019-20

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations 2018 notified by the Council vide notification number F.No.AB/AICTE/REG/2018 dated 31/12/2018 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Permanent Id	1-2145671	**Application Id**	1-4261715485
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	**Name of the Society/Trust**	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203	**Society/Trust Address**	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institute Type	Unaided - Private	**Region**	South-West

Opted for Change from Women to Co-Ed and vice versa	No	**Change from Women to Co-Ed and vice versa Approved or Not**	NA
Opted for Change of Name	No	**Change of Name Approved or Not**	NA
Opted for Change of Site/Location	No	**Change of Site/Location Approved or Not**	NA
Opted for Conversion from Degree to Diploma or vice versa	No	**Conversion for Degree to Diploma or vice versa Approved or Not**	NA
Opted for Organization Name Change	No	**Change of Organization Name Approved or Not**	NA
Opted for Merger of Institution	No	**Merger of Institution Approved or Not**	NA
Opted for Introduction of New Program/Level	No	**Introduction of Program/Level Approved or Not**	NA

To conduct following Courses with the Intake indicated below for the Academic Year 2019-20

Program	Shift	Level	Course	FT/PT+	Affiliating Body (Univ/Body)	Intake Approved for 2019-20	NRI Approval Status	PIO / FN / Gulf quota/ OCI/ Approval Status
MANAGEMENT	1st	POST GRADUATE	MASTERS IN BUSINESS ADMINISTRATIO	FT	Visvesvaraya Technological University, Belgaum	60	NA	NA

			N					
ENGINEERING AND TECHNOLOGY	1st	UNDER GRADUATE	MECHANICAL ENGINEERING	FT	Visvesvaraya Technological University, Belgaum	90	NA	NA
ENGINEERING AND TECHNOLOGY	1st	UNDER GRADUATE	CIVIL ENGINEERING	FT	Visvesvaraya Technological University, Belgaum	60	NA	NA
ENGINEERING AND TECHNOLOGY	1st	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	FT	Visvesvaraya Technological University, Belgaum	90	NA	NA
ENGINEERING AND TECHNOLOGY	1st	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	FT	Visvesvaraya Technological University, Belgaum	120	NA	NA

+FT –Full Time,PT-Part Time

Punitive Action against the Institute

Course(s) Applied for Closure by the Institute for the Academic Year 2019-20

Program	Shift	Level	Course	FT/PT+	Affiliating Body (Univ/Body)	Course Closure Status
ENGINEERING AND TECHNOLOGY	1st	POST GRADUATE	DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS	FT	Visvesvaraya Technological University, Belgaum	Approved

+FT-Full Time,PT-Part Time

In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Strict compliance of Anti-Ragging Regulation: - Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 37-3/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

It is mandatory to comply all the essential requirements as given in APH 2019-20(appendix 6)

NOTE: If the State Government / UT / DTE / DME has a reservation policy for admission in Technical Education Institutes and the same is applicable to Private & Self-financing Technical Institutions, then the State Government / UT/ DTE / DME shall ensure that 10 % of Reservation for EWS would be operational from the Academic year 2019-20 without affecting the percentage reservations of SC/ST/OBC/General . However, this would not be applicable in the case of Minority Institutions referred to the clause (1) of Article 30 of Constitution of India.

Prof. A.P Mittal
Member Secretary, AICTE

Copy to:

1. **The Director Of Technical Education**, Karnataka**

2. **The Registrar**,**
   Visvesvaraya Technological University, Belgaum

3. **The Principal / Director,**
   Vivekananda College Of Engineering And Technology
   Neharu Nagara

Puttur Taluk
Dakshina Kannada
Karnataka
574203,
Puttur,Dakshina Kannada,
Karnataka,574203

4. **The Secretary / Chairman,**
Vivekananda Vidyavardhaka Sangha Puttur (R)
Vivekananda College Campus
Neharu Nagara.
Puttur,D Kannada(Dk),
Karnataka,574203

5. **The Regional Officer,**
All India Council for Technical Education
Health Centre Building
Bangalore University Campus
Bangalore - 560 009, Karnataka

6. **Guard File(AICTE)**

Note: Validity of the Course details may be verified at http://www.aicte-india.org/

****** Individual Approval letter copy will not be communicated through Post/Email. However, consolidated list of Approved Institutions(bulk) will be shared through official Email Address to the concerned Authorities mentioned above.

All India Council for Technical Education

(A Statutory body under Ministry of HRD, Govt. of India)

Nelson Mandela Marg,Vasant Kunj, New Delhi-110070 Website: www.aicte-india.org

APPROVAL PROCESS 2020-21

Extension of Approval (EoA)

F.No. South-West/1-7004809224/2020/EOA Date: 15-Jun-2020

To,

The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of Approval for the Academic Year 2020-21

Ref: Application of the Institution for Extension of Approval for the Academic Year 2020-21

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations 2020 notified by the Council vide notification number F.No. AB/AICTE/REG/2020 dated 4th February 2020 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Permanent Id	1-2145671	**Application Id**	1-7004809224
Name of the Institute	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	**Name of the Society/Trust**	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
Institute Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203	**Society/Trust Address**	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institute Type	Private-Self Financing	**Region**	South-West

To conduct following Courses with the Intake indicated below for the Academic Year 2020-21

Program	Level	Course	Affiliating Body (University /Body)	Intake Approved for 2019-20	Intake Approved for 2020-21	NRI Approval Status	PIO / FN / Gulf quota/ OCI/ Approval Status
MANAGEMENT	POST GRADUATE	MBA	Visvesvaraya Technological University, Belgaum	60	60	NA	NA
ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	MECHANICAL ENGINEERING	Visvesvaraya Technological University, Belgaum	90	60	NA	NA
ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	CIVIL ENGINEERING	Visvesvaraya Technological University, Belgaum	60	60	NA	NA

ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	Visvesvaraya Technological University, Belgaum	90	90	NA	NA
ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	Visvesvaraya Technological University, Belgaum	120	120	NA	NA
ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING	Visvesvaraya Technological University, Belgaum	0	60##$$	NA	NA

Approved New Course(s)
$$ Course(s) should be offered in Emerging Area

It is mandatory to comply with all the essential requirements as given in APH 2020-21 (Appendix 6)

Important Instructions

1. The State Government/ UT/ Directorate of Technical Education/ Directorate of Medical Education shall ensure that 10% of reservation for Economically Weaker Section (EWS) as per the reservation policy for admission, operational from the Academic year 2020-21 is implemented without affecting the reservation percentages of SC/ ST/ OBC/ General. However, this would not be applicable in the case of Minority Institutions referred to the Clause (1) of Article 30 of Constitution of India. Such Institution shall be permitted to increase in annual permitted strength over a maximum period of two years beginning with the Academic Year 2020-21

2. The Institution offering courses earlier in the Regular Shift, First Shift, Second Shift/Part Time now amalgamated as total intake shall have to fulfil all facilities such as Infrastructure, Faculty and other requirements as per the norms specified in the Approval Process Handbook 2020-21 for the Total Approved Intake. Further, the Institutions Deemed to be Universities/ Institutions having Accreditation/ Autonomy status shall have to maintain the Faculty: Student ratio as specified in the Approval Process Handbook. All such Institutions/ Universities shall have to create the necessary Faculty, Infrastructure and other facilities WITHIN 2 YEARS to fulfil the norms based on the Affidavit submitted to AICTE.

3. In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

4. Strict compliance of Anti-Ragging Regulation: - Approval is subject to strict compliance of provisions made in AICTE Regulation notified vide F. No. 373/Legal/AICTE/2009 dated July 1, 2009 for Prevention and Prohibition of Ragging in Technical Institutions. In case Institution fails to take adequate steps to Prevent Ragging or fails to act in accordance with AICTE Regulation or fails to punish perpetrators or incidents of Ragging, it will be liable to take any action as defined under clause 9(4) of the said Regulation.

Prof.Rajive Kumar
Member Secretary, AICTE

Copy to:

1. **The Director Of Technical Education**, Karnataka**

2. **The Registrar**,**
   Visvesvaraya Technological University, Belgaum

3. **The Principal / Director,**
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY

Neharu Nagara
Puttur Taluk
Dakshina Kannada
Karnataka
574203,
Puttur,Dakshina Kannada,
Karnataka,574203

4. **The Secretary / Chairman,**
VIVEKANANDA COLLEGE CAMPUS
NEHARU NAGARA
PUTTUR,D KANNADA(DK)
Karnataka,574203

5. **The Regional Officer,**
All India Council for Technical Education
Health Centre Building
Bangalore University Campus
Bangalore - 560 009, Karnataka

6. **Guard File(AICTE)**

Note: Validity of the Course details may be verified at http://www.aicte-india.org/

****** Individual Approval letter copy will not be communicated through Post/Email. However, consolidated list of Approved Institutions(bulk) will be shared through official Email Address to the concerned Authorities mentioned above.

All India Council for Technical Education

(A Statutory body under Ministry of Education, Govt. of India)

Nelson Mandela Marg,Vasant Kunj, New Delhi-110070 Website: www.aicte-india.org

APPROVAL PROCESS 2021-22

Extension of Approval (EoA)

F.No. South-West/1-9319473714/2021/EOA Date: 15-Jul-2021

To,

The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of Approval for the Academic Year 2021-22

Ref: Application of the Institution for Extension of Approval for the Academic Year 2021-22

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Education) (1st Amendment) Regulations, 2021 notified on 24th February 2021 and other notifications as applicable and published from time to time, I am directed to convey the approval to

Permanent Id	1-2145671	**Application Id**	1-9319473714
Name of the Institution /University	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	**Name of the Society/Trust**	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
Institution /University Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203	**Society/Trust Address**	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institution /University Type	Private-Self Financing	**Region**	South-West

Opted for Introduction of New Program/Level	Yes	**Introduction of Program/Level Approved or Not**	Approved

To conduct following Programs / Courses with the Intake indicated below for the Academic Year 2021-22

Program	Level	Course	Affiliating Body (University /Body)	Intake Approved for 2020-21	Intake Approved for 2021-22	NRI Approval Status	FN / Gulf quota/ OCI/ Approval Status
MANAGEMENT	POST GRADUATE	MBA	Visvesvaraya Technological University, Belgaum	60	60	No	No
ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	MECHANICAL ENGINEERING	Visvesvaraya Technological University, Belgaum	60	30	No	No

ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	CIVIL ENGINEERING	Visvesvaraya Technological University, Belgaum	60	30	No	No
ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	ELECTRONICS AND COMMUNICATIONS ENGINEERING	Visvesvaraya Technological University, Belgaum	90	60	No	No
ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING	Visvesvaraya Technological University, Belgaum	120	120	No	No
ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING	Visvesvaraya Technological University, Belgaum	60	60	No	No
MCA	POST GRADUATE	MASTER OF COMPUTER APPLICATIONS	Visvesvaraya Technological University, Belgaum	0	60##	No	No
ENGINEERING AND TECHNOLOGY	UNDER GRADUATE	COMPUTER SCIENCE AND ENGINEERING (DATA SCIENCE)	Visvesvaraya Technological University, Belgaum	0	60##	No	No

Approved New Course(s)

It is mandatory to comply with all the essential requirements as given in APH 2021-22 (Appendix 6)

Important Instructions

1. The State Government/ UT/ Directorate of Technical Education/ Directorate of Medical Education shall ensure that 10% of reservation for Economically Weaker Section (EWS) as per the reservation policy for admission, operational from the Academic year 2019-20 is implemented without affecting the reservation percentages of SC/ ST/ OBC/ General. However, this would not be applicable in the case of Minority Institutions referred to the Clause (1) of Article 30 of Constitution of India. Such Institution shall be permitted to increase in annual permitted strength over a maximum period of two years.

2. The Institution offering courses earlier in the Regular Shift, First Shift, Second Shift/Part Time now amalgamated as total intake shall have to fulfil all facilities such as Infrastructure, Faculty and other requirements as per the norms specified in the Approval Process Handbook 2021-22 for the Total Approved Intake. Further, the Institutions Deemed to be Universities/ Institutions having Accreditation/ Autonomy status shall have to maintain the Faculty: Student ratio as specified in the Approval Process Handbook.

3. Strict compliance of Anti-Ragging Regulation, Establishment of Committee for SC/ ST, Establishment of Internal Complaint Committee (ICC), Establishment of Online Grievance Redressal Mechanism, Barrier Free Built Environment for disabled and elderly persons, Fire and Safety Certificate should be maintained as per the provisions made in Approval Process Handbook and AICTE Regulation notified from time to time.

4. In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Prof.Rajive Kumar
Member Secretary, AICTE

Copy ** to:

1. **The Director of Technical Education**, Karnataka**

2. **The Registrar**,**
   Visvesvaraya Technological University, Belgaum

3. **The Principal / Director,**
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
   Neharu Nagara
   Puttur Taluk
   Dakshina Kannada
   Karnataka
   574203,
   Puttur,Dakshina Kannada,
   Karnataka,574203

4. **The Secretary / Chairman,**
   VIVEKANANDA COLLEGE CAMPUS
   NEHARU NAGARA
   PUTTUR,D KANNADA(DK)
   Karnataka,574203

5. **The Regional Officer,**
   All India Council for Technical Education
   Health Centre Building
   Bangalore University Campus
   Bangalore - 560 009, Karnataka

6. **Guard File(AICTE)**

Note: Validity of the Course details may be verified at http://www.aicte-india.org/ .

****** Individual Approval letter copy will not be communicated through Post/Email. However, consolidated list of Approved Institutions(bulk) will be shared through official Email Address to the concerned Authorities mentioned above.

This is a computer generated Statement. No signature Required

All India Council for Technical Education

(A Statutory body under Ministry of Education, Govt. of India)

Nelson Mandela Marg,Vasant Kunj, New Delhi-110070 Website: www.aicte-india.org

APPROVAL PROCESS 2022-23

Extension of Approval (EoA)

F.No. South-West/1-10975684720/2022/EOA Date: 03-Jun-2022

To,

The Principal Secretary (Hr. & Tech Education)
Govt. of Karnataka, K. G.S., 6th Floor,
M.S. Building, R. N. 645,Dr. B. R. Ambedkar Road,
Bangalore-560001

Sub: Extension of Approval for the Academic Year 2022-23

Ref: Application of the Institution for Extension of Approval for the Academic Year 2022-23

Sir/Madam,

In terms of the provisions under the All India Council for Technical Education (Grant of Approvals for Technical Institutions) Regulations, 2022 Notified on 4th February, 2022 and amended on 24th February 2022 and norms standards, procedures and conditions prescribed by the Council from time to time, I am directed to convey the approval to

Permanent Id	1-2145671	**Application Id**	1-10975684720
Name of the Institution	VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY	**Name of the Society/Trust**	VIVEKANANDA VIDYAVARDHAKA SANGHA PUTTUR (R)
Institution Address	NEHARU NAGARA PUTTUR TALUK DAKSHINA KANNADA KARNATAKA 574203, PUTTUR, DAKSHINA KANNADA, Karnataka, 574203	**Society/Trust Address**	VIVEKANANDA COLLEGE CAMPUS NEHARU NAGARA,PUTTUR,D KANNADA(DK),Karnataka,574203
Institution Type	Private-Self Financing	**Region**	South-West
Year of Establishment	2001		

To conduct following Courses with the Intake indicated below for the Academic Year 2022-23

Level	Program	Course	Affiliating Body (University /Body)	Intake Approved for 2021-22	Intake Approved for 2022-23	NRI Approval Status	FN / Gulf quota/ OCI/ Approval Status
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING	Visvesvaraya Technological University, Belgaum	60	60	NA	NA
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	CIVIL ENGINEERING	Visvesvaraya Technological University, Belgaum	30	30	NA	NA
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	COMPUTER SCIENCE AND ENGINEERING	Visvesvaraya Technological University, Belgaum	120	120	NA	NA

Level	Program	Course	Affiliating Body (University /Body)	Intake Approved for 2021-22	Intake Approved for 2022-23	NRI Approval Status	FN / Gulf quota/ OCI/ Approval Status
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	COMPUTER SCIENCE AND ENGINEERING (DATA SCIENCE)	Visvesvaraya Technological University, Belgaum	60	60	NA	NA
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	ELECTRONICS AND COMMUNICATION ENGINEERING	Visvesvaraya Technological University, Belgaum	60	60	NA	NA
UNDER GRADUATE	ENGINEERING AND TECHNOLOGY	MECHANICAL ENGINEERING	Visvesvaraya Technological University, Belgaum	30	30	NA	NA
POST GRADUATE	MANAGEMENT	MBA	Visvesvaraya Technological University, Belgaum	60	60	NA	NA
POST GRADUATE	MCA	MASTER OF COMPUTER APPLICATIONS	Visvesvaraya Technological University, Belgaum	60	60	NA	NA

It is mandatory to comply with all the essential requirements as given in APH 2022-23 (Appendix 6)

Important Instructions

1. The State Government/ UT/ Directorate of Technical Education/ Directorate of Medical Education shall ensure that 10% of reservation for Economically Weaker Section (EWS) as per the reservation policy for admission, operational from the Academic year 2019-20 is implemented without affecting the reservation percentages of SC/ ST/ OBC (NCL)/ General. However, this would not be applicable in the case of Minority Institutions referred to the Clause (1) of Article 30 of Constitution of India. Such Institution shall be permitted to increase in annual permitted strength over a maximum period of two years.

2. The Institution offering courses earlier in the Regular Shift, First Shift, Second Shift/Part Time are now amalgamated as total intake and shall have to fulfil all facilities such as Infrastructure, Faculty and other requirements as per the norms specified in the Approval Process Handbook 2022-23 for the Total Approved Intake. Further, the Institutions Deemed to be Universities/ Institutions having Accreditation/ Autonomy status shall have to maintain the Faculty: Student ratio as specified in the Approval Process Handbook. All such Institutions/ Universities shall have to create the necessary Faculty, Infrastructure and other facilities WITHIN 2 YEARS to fulfil the norms based on the Affidavit submitted to AICTE beginning with the Academic Year 2022-23

3. Strict compliance of Anti-Ragging Regulation, Establishment of Committee for SC/ ST, Establishment of Internal Complaint Committee (ICC), Establishment of Online Grievance Redressal Mechanism, Barrier Free Built Environment for disabled and elderly persons, Fire and Safety Certificate should be maintained as Approval Process Handbook and provisions made in AICTE Regulation notified from time to time.

4. In case of any differences in content in this Computer generated Extension of Approval Letter, the content/information as approved by the Executive Council / General Council as available on the record of AICTE shall be final and binding.

Pharmacy Institute: In compliance with the order dated 05.03.2020 passed by the Hon'ble Supreme Court of India in Transferred Petitions (CIVIL) No 87-101 of 2014, for the existing institutions offering courses in Pharmacy Programme, approval of Pharmacy Council of India (PCI) is mandatory and AICTE approval is NOT required. The requirements for running the Programme (Diploma / UG / PG) such as Land & Build-up Area, Student-faculty ratio, Intake etc. will be as per the respective regulatory body (PCI).
In case of any inconsistency in the course name and intake for EoA issued by AICTE and the approval by PCI, the approval of PCI shall prevail.

Architecture Institute: In compliance with the order dated 08.11.2019 passed by the Hon'ble Supreme Court of Indian CA No.364/ 2005, for the existing Institutions offering Courses in Architecture Programme, approval by the Council of Architecture (CoA) is mandatory and AICTE approval is NOT required. The requirements for running the Programme (Diploma / UG / PG) such as Land & Build-up Area, Student-faculty ratio, Intake etc. will be as per respective regulatory body (CoA). In case of any inconsistency in the course name and intake for EoA issued by AICTE and the approval by CoA, the approval of CoA shall prevail.

Deemed to be University: Institutions Deemed to be Universities (Running Technical Education Programmes), it is mandatory to have AICTE approval from the Academic Year 2018-19 in compliance of the Hon'ble Supreme Court Order dated 03-11-2017 passed in CA No.17869- 17870 /2017.

Prof.Rajive Kumar
Member Secretary, AICTE

Copy to:

1. **The Director Of Technical Education**, Karnataka**

2. **The Registrar**,**
   Visvesvaraya Technological University, Belgaum

3. **The Principal / Director,**
   VIVEKANANDA COLLEGE OF ENGINEERING AND TECHNOLOGY
   Neharu Nagara
   Puttur Taluk
   Dakshina Kannada
   Karnataka
   574203,
   Puttur,Dakshina Kannada,
   Karnataka,574203

4. **The Secretary / Chairman,**
   VIVEKANANDA COLLEGE CAMPUS
   NEHARU NAGARA
   PUTTUR,D KANNADA(DK)

Karnataka,574203

5. **The Regional Officer,**
All India Council for Technical Education
Health Centre Building
Bangalore University Campus
Bangalore - 560 009, Karnataka

6. **Guard File(AICTE)**

Note: Validity of the Course details may be verified at http://www.aicte-india.org/

****** Individual Approval letter copy will not be communicated through Post/Email. However, consolidated list of Approved Institutions(bulk) will be shared through official Email Address to the concerned Authorities mentioned above.

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